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Verification of CDM circuit simulation using an ESD evaluation circuit

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Abstract

In this work, the capability of circuit simulation to predict CDM robustness of integrated circuits and to determine weak circuit elements is studied. The applicability is demonstrated for an ESD evaluation circuit designed to enable the analysis and optimization of ESD protection strategies in an early design phase during the introduction of a new technology. CDM circuit simulation is compared to the measurement results of variations of this circuit in two different package types. Failure locations are verified with physical failure analysis. The failure locations and CDM failure levels were reproduced accurately with circuit simulation for all circuit and package variations.

1. Introduction

Due to technology scaling and expansion of automated handling, failures in ICs caused by Charged Device Model (CDM) ESD are an increasingly important reliability issue. Even today, a significant portion of ESD field returns is due to damages originating from CDM stress. Moreover, CDM discharges can cause latent damages which could degrade and eventually lead to definite failure of the IC.

Discovering and correcting weak circuit elements before silicon is available is necessary to optimize ESD protection strategies and assure product reliability. Hence, research in the past has dealt with the ability to determine the behavior of ICs during CDM discharges with circuit simulation. Several studies investigate CDM behavior on device level [1–4] and for input circuits and test structures [4–7]. Addressing chip level simulation of CDM discharges, Lee et al. [8] suggest that the probability of gate oxide rupture is correlated with the package capacitance of connected circuit parts. The authors propose a CDM simulation method to roughly predict the most probable CDM failure location for failure analysis. Brennan et al. [9] introduced design tools for ensuring robust ESD protection in an early design stage. The authors demonstrate the applicability of the introduced tools for achieving high CDM robustness for test products in different technologies. Cross-checks evaluating the impact of the implemented improvements are not presented.

Simulation of CDM ESD events is a challenging task. Parasitic effects play an important role during the discharge, the occurring fast transients and the short nature of the event make it hard to comprehend. Therefore, it is often difficult to determine if the simulated behavior corresponds to the actual physical behavior of the circuit. Hence, the main intention of our work is to verify the applicability and accuracy of the proposed CDM circuit simulation method. For this purpose, variations of an ESD evaluation circuit in two package types are used. Detailed cross-checks between CDM measurements of the different test devices and the results derived from circuit simulation are carried out. Failure Analysis (FA) is performed for all variations to confirm failure modes and locations.

For evaluation of the proposed CDM circuit simulation method, the impact of including parasitic elements in the

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simulation setup, such as interconnect resistance and capacitance, is investigated. A previous study [7] demonstrated the importance of taking the substrate into account for achieving correct CDM simulation results. Hence, in contrast to prior chip level CDM simulation studies, the substrate is accounted for in the simulation and the impact of the substrate is confirmed in this work. Furthermore, the importance of using modified and extended device models for CDM circuit simulation is shown as devices can be biased into unintended operating modes during CDM discharges, which are not covered by standard compact device models.

Another challenge of protecting ICs from damage caused by CDM ESD is that the behavior of ICs during the discharge strongly depends on the package type, the design and especially the applied technology. Consequently, designs are typically optimized for CDM ESD by applying experience resulting from previous or comparable designs in the same technology. In previous studies, the ESD protection concept had already been established for the investigated technology and was optimized for a specific design. Another important motivation of this work is to establish a method to optimize CDM ESD protection concepts in the early design phase after the introduction of a new technology. Therefore, the evaluation circuit was implemented, including variations of CDM relevant properties. ESD protection concepts are optimized and weak circuit elements determined by applying the results from CDM tests at the proposed evaluation circuit. For further optimization of CDM robustness and the evaluation of variations of the protection concept, the introduced and verified CDM circuit simulation method can be applied.

This paper is organized as follows: The next section introduces the ESD evaluation circuit which was used for the study and presents the respective CDM measurement results. Section 3 investigates the influence of the substrate and parasitic elements on CDM simulation results and proposes a simulation setup suitable for transient CDM simulation. In Section 4, the simulation results are verified by comparison to CDM measurements and physical failure analysis results. In the final section we summarize the results of our work.

2. CDM ESD evaluation circuit

2.1. Circuit description

An evaluation circuit (EC) was designed that serves two main purposes. It is applied to verify the ability of circuit simulation to predict circuits' weak elements for CDM ESD stress. Also, it is used for investigating the quality of CDM ESD protection strategies in newly introduced technologies. A schematic description of the circuit is depicted in Fig. 1. This design is simple enough to make circuit simulation feasible, but includes many typical characteristics of a complete IC, such as different power and ground domains and long interconnect lines with the related parasitic resistance and capacitance. Hence, the conclusions achieved from this circuit are expected to be generally applicable.

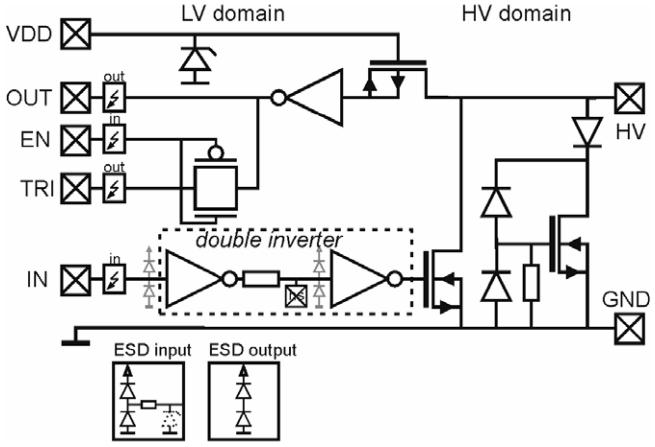

Fig. 1. Principle schematic of investigated CDM ESD evaluation circuit. The secondary diode in the input ESD protection (dotted) is only included in variation ECD_P. In variation ECR_M gate protection diodes are added (grey). The pad between the two inverters, which was placed there for analysis of the electrical characteristic, was not stressed during the CDM test.

As already mentioned, the circuit was mainly designed for the purpose of evaluating the feasibility of CDM circuit simulation. Achieving an especially high CDM robustness of the evaluation circuit was not the aim, since this would have delimitated its applicability to verify the simulation method. In addition to that, the technology was relatively new at the time the circuit was implemented and therefore the CDM robustness of this technology was not known. As a consequence, the circuit was designed to be more delicate. Two variations of the evaluation circuit were implemented with modifications of the recommended standard ESD protection for the applied technology. One circuit was designed to be very delicate (EC Delicate – ECD) for CDM stress, one to be slightly more robust (EC Robust – ECR). Variation ECR is packaged in a MQFP package with 64 Pins (ECR_M). To investigate the influence of the package on measurement results and the correct reproduction by circuit simulation, ECD is packaged in two different package types, PowerSO36 (ECD_P) and MQFP64 (ECD_M). Due to a deviation in the bonding diagram, variation ECD_P includes an additional protection diode compared to ECD_M.

2.2. CDM measurement results

The evaluation circuits were measured with a CDM tester according to the ESDA standard with field induced charging. All input, output, power and ground pins were stressed in one test cycle. The CDM discharge current was recorded for each pin and test cycle. To enable the differentiation of failure modes, only one stress polarity was applied to each device. After each test cycle, functional