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Research note

Critical dimension control in photolithography based on the yield by a simulation program

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Abstract

The critical dimension (CD) of wafers in photolithography is the most important parameter that determines the final performance of devices. The sampling of CD's, as a result, is essential and must be taken with caution. Process yield is a common criterion used in the manufacturing industry for measuring process performance. A measurement index, called S_{pk}, has been proposed to calculate the yield for normal processes, and can be used to establish the relationship between the manufacturing specifications and the actual process performance, which provides an exact measure on process yield. In this paper, we solve the CD control problem based on the yield index S_{pk}. The critical values required for the hypothesis testing, using the standard simulation technique, for various commonly used performance requirements, are obtained. Extensive simulation results are provided and analyzed. The results indicate that a sample size greater than 145 is sufficient to ensure that the decisions made are insensitive to the process precision and the process accuracy. The investigation is useful to the practitioners for making reliable decisions in testing process performance of a stepper and quality of an engineering lot by CD control.

1. Introduction

A trend of semiconductor industry is to manufacture integrated circuits (ICs) with smaller devices and feature sizes on wafers of larger diameters. The progressively more demanding specifications and shrunken device size put a tremendous pressure on process control, especially the control of photolithography.

In photolithography, the pattern printed on a wafer is not an exact replica of the mask pattern in practice. "Critical-dimension," or just "CD," is defined as the linewidth of the photoresist (PR) line printed on a wafer and reflects whether the exposure and development are proper to produce geometries of the correct size [1]. Because of limited resources and more-stabilized advanced process system, the sample size of CDs is shrinking. Therefore, the goal of this paper is to find the most suitable number of chips that should be selected in each lot (25 pieces) of wafers for measuring CD's in such instance. The rest of the paper is organized as follows. Section 2 discusses the importance of CD control in photolithography. Process yield and yield measurement index, S_{pk}, are briefly introduced in Section 3. Section 4 presents the simulation for the critical values of S_{pk}.

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Section 5 presents an application example and solves the number of samples required for checking the stability of a stepper or the quality of an engineering lot. Some conclusion remarks are made in the last section.

2. Control of the photolithography process by CD measurement

Photolithography, taking about 40–50% of the total wafer-processing time, is the core of the IC manufacturing process, which requires six to eight weeks to fabricate bare wafers into finished wafers [2]. Photolithography requires high resolution, high sensitivity, precise alignment and low defect density, and an advanced IC chip usually needs more than 30 patterning steps of which each one must align with the previous one precisely to successfully transfer the pattern of the chip design.

Three major steps of the photolithography are PR coating, alignment and exposure, and developing. The most critical step of the process is alignment and exposure, which determines the success of transforming the IC design pattern on the mask or reticle to the PR on the wafer surface [2]. The last step of the photolithography process is after-develop-inspection, which determines whether the steps up to this point have been performed correctly and within the specified tolerance and whether the photolithography produced a satisfactory pattern on the PR [3]. Pattern inspection is essential since the wafers that fail to pass the inspection can still be sent to strip the PR and to rework on the whole process again. However, after a wrong pattern is etched or implanted, it is almost impossible to rework a wafer then. As a result, the inspection process is very important to detect whether the pattern on the PR is misaligned, whether there are incorrect critical dimensions (CD's) and whether there are surface irregularities [2]. In advanced IC fabs, CD loss, caused mainly by overexposure or over-development, lead to the most photolithography reworks. Therefore, a successful CD control is essential for the final performance of the devices and the achievement of throughput and profit target of a firm.

To control the process effectively, CD measurements must be made on each layer in the manufacturing process, which typically contains 10–15 such layers [4]. The CD can be measured at the top, bottom or any height of the resist profile [1]. For the new generation of ICs which have submicron features made on step-and-repeat printers using die-by-die alignment, the measurement task is becoming more and more pressing and difficult [4].

CDs are usually measured from bar grating patterns, and the measurement is generated by comparing the bar diameter to the space between bars which should be equal [4]. The difficulty with this method is to determine where the edges of a bar are in the intensity profile especially when ringing from interference fringes is present. Generally, an arbitrary point on the curve that gives the most repeatable results is selected since process control in repeatability usually takes priority over absolute precision [4]. Automated systems for CD measurement are common nowadays, and the inspection data generated from the systems is further analyzed to determine the acceptability of wafers.

The distribution of CDs is referred to as across chip linewidth variation (ACLV), and the width of the distribution is represented by 3σ, where σ is the standard deviation of a normal or close to normal distribution [5]. Because the statistical sampling is often too small to examine the normality of the distribution, the distribution width is usually expressed by total indicated range (TIR), the difference between the maximum CD and minimum CD in a sample. Statistical methodologies like Shewhart-type control charts are usable tools in practice to check if CDs are in or out of statistical control [6]. However, more precise analysis with designed experimental datasets is often required to deal with CD variation because significant CD variation may need prompt decisions such as mask revisions and process conditions changes, and techniques, for example, the analysis of variance (ANOVA), are often utilized to investigate CD variation [6].

3. An overview of the process yield and yield measurement index S_{pk}

Process yield, the percentage of processed product unit passing the inspection, is a common and basic criterion used in the manufacturing industry as a numerical measure on process performance. For a product to pass the inspection, its product characteristic must fall within the manufacturing tolerance, and all passed product units are equally accepted by the producer. On the other hand, for a product that is rejected due to nonconformities, it may be scrapped, or additional cost is required to repair the product. The process yield, for a process with two-sided manufacturing specifications, can be expressed as $F(\mathrm{USL}) - F(\mathrm{LSL})$, where USL and LSL are the upper and the lower specification limits, respectively, and $F(\cdot)$ is the cumulative distribution function of the process characteristic [7]. For a process characteristic following a normal distribution, the process yield is $\Phi[(\mathrm{USL} - \mu)/\sigma] - \Phi[(\mu - \mathrm{LSL})/\sigma]$, where μ is the process mean, σ is the process standard deviation, and $\Phi(\cdot)$ is the cumulative distribution function of the standard normal distribution $N(0,1)$ [7].

Process capability indices (PCIs) establish the relationship between the actual process performance and the manufacturing specifications. An abundant literature