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TARGET 5: A new multi-channel digitizer with triggering capabilities for gamma-ray atmospheric Cherenkov telescopes

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ABSTRACT

TARGET 5 is a new application-specific integrated circuit (ASIC) of the TARGET family, designed for the readout of signals from photosensors in the cameras of imaging atmospheric Cherenkov telescopes (IACTs) for ground-based gamma-ray astronomy. TARGET 5 combines sampling and digitization on 16 signal channels with the formation of trigger signals based on the analog sum of groups of four channels. We describe the ASIC architecture and performance. TARGET 5 improves over the performance of the first-generation TARGET ASIC, achieving: tunable sampling frequency from $<$0.4 GSa/s to $>$1 GSa/s; a dynamic range on the data path of 1.2 V with effective dynamic range of 11 bits and DC noise of $\sim$0.6 mV; 3-dB bandwidth of 500 MHz; crosstalk between adjacent channels $<$1.3%; charge resolution improving from 40% to $<$4% between 3 photoelectrons (p.e.) and $>$100 p.e. (assuming 4 mV per p.e.); and minimum stable trigger threshold of 20 mV (5 p.e.) with trigger noise of 5 mV (1.2 p.e.), which is mostly limited by interference between trigger and sampling operations. TARGET 5 is the first ASIC of the TARGET family used in an IACT prototype, providing one development path for readout electronics in the forthcoming Cherenkov Telescope Array (CTA).

1. Introduction

In the past three decades, imaging atmospheric Cherenkov telescopes (IACTs) have greatly advanced observations of very-high-energy gamma-ray emission from the Universe, with numerous implications for astrophysics, particle physics, and cosmology [e.g., 1]. The advent of the Cherenkov Telescope Array (CTA) [2] will bring a revolution to this field. CTA will increase the source sensitivity by an order of magnitude at energies from 100 GeV to 10 TeV and will extend observations to the ranges well below 100 GeV and above 100 TeV.

The requirements of CTA drive innovation to improve performance and lower cost. One innovative design is the Schwarzschild–Couder telescope [3], which features dual-mirror optics for better optical performance (focusing of Cherenkov photons) and a reduced camera size compared to the traditional single-mirror (Davies-Cotton) design used so far for IACTs. The reduced camera size enables compact, inexpensive, densely pixelated photodetectors such as silicon photomultipliers. The optical performance combined with dense pixelation is expected to improve field of view, angular resolution, and hadronic background rejection capabilities [4].

TARGET is an application-specific integrated circuit (ASIC) series that has been designed for the processing of the photodetector signals in such telescopes. The goals in the inception of TARGET were to keep the costs low and integrate several functionalities in

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a compact design. We have described the concept of TARGET 1, the first generation of ASICs of the TARGET family, and characterized its performance in [5]. Several improvements drove the development of TARGET 5 (after a few design iterations), which is described in this paper.

TARGET 5 is the first chip of the TARGET family to be used in a telescope prototype, namely a prototype of the Gamma-ray Cherenkov Telescope (GCT) [6], a Schwarzschild–Couder small-sized telescope proposed for the CTA project. TARGET 5 is used in the first prototype of the GCT camera, also known as Compact High Energy Camera with MAPMTs (CHEC-M) [7,8]. TARGET is also planned to be used in a medium-sized telescope proposed in the framework of the CTA project, namely the Schwarzschild-Couder Telescope (SCT) [9].

Key features of TARGET are:

- a compact design that combines signal sampling and digitization, as well as triggering, for 16 channels in a single chip, which lowers the cost,[1] improves on reliability further reducing maintenance costs, and enables its use with compact photodetectors such as multi-anode photomultiplier tubes (MAPMTs) or silicon photomultipliers in a compact camera design
- a sampling frequency tunable up to >1 GSa/s, ideally suited for the measurement of the $\gtrsim 5$ ns pulses from Cherenkov flashes
- a deep buffer (16,384 samples in TARGET 5) for large trigger latency tolerance between distant ($\sim$1 km) telescopes[2]
- dynamic range >10 bits
- moderate power consumption, for the applications described in this paper $\lesssim 20$ mW per channel

TARGET ASICs are implemented for IACTs into front-end electronics modules that combine all the functions described above to read out 64 photodetector pixels using six or fewer printed circuit boards, four ASICs, and a companion field-programmable gate array (FPGA) [5]. The low number of components supports affordability and reliability.

The structure of this paper is as follows. Section 2 describes the architecture of the TARGET 5 ASIC. Section 3 presents the characterization of its performance, including sampling and digitization in Section 3.2, as well as triggering in Section 3.3. Section 4 briefly outlines how TARGET 5 is implemented into front-end electronics modules for CHEC-M, and Section 5 presents the conclusions and outlook.

2. The TARGET 5 architecture

Fig. 1 presents an overview of the major functional blocks of the TARGET 5 ASIC: triggering, analog sampling and storage, analog-to-digital converters (ADC), and configuration of control features and digital-to-analog converters (DAC) provided via a serial-parallel interface. The general features of TARGET 5 detailed in the following text are summarized in Table 1 with comparison to TARGET 1.

As with TARGET 1 and other predecessors in the TARGET family, TARGET 5 is a 16-channel device where both a signal and its reference signal (an input pedestal voltage, `Vped`) are input to the ASIC, to provide a modest amount of common-mode noise rejection, as well as reference for the trigger gain path. The input signal is simultaneously processed for sampling (data path) and triggering (trigger path).

ASICs of the TARGET family use switched capacitor arrays (SCAs) to sample signals at very high sampling rate, i.e., the input is connected to an array of capacitors via analog switches which are sequentially connected and disconnected to sample the signal at regular intervals.

The sampling buffer depth ($\sim$16 µs) needed to trigger using coincidence between distant (up to 1 km) telescopes requires several thousand storage capacitors given a sampling frequency of 1 GSa/s. Directly driving the capacitance of such an array limits its analog bandwidth. Therefore, one of the major improvements of TARGET 5 over TARGET 1 is the separation of sampling operations into two stages in order to simultaneously achieve large bandwidth and a deep buffer for trigger decisions. In the first stage, an SCA with a small number of cells (two blocks of 32 cells), called the sampling array, is used for signal sampling in order to reduce the capacitance load on the input. In the second stage, the samples are transferred to an SCA with a large number of cells (16,348), called the storage array, which provides the desired buffer depth. While acquisition occurs in one group of 32 cells in the sampling array, the other is written to the storage array. This ping-pong approach provides continuous sampling.

Control of the sample timing is provided by a timebase generator that is driven by two digital signals sent from the FPGA to the ASIC: `SSTin` and `SSPin`. These signals go through time delay elements that are current-starved inverters and control charge tracking and hold in the SCAs. The sampling speed of TARGET 5 is controlled by adjusting the supply current for the inverter in the delay elements.

Previous measurements of our timebase generator indicated that the sampling speed is temperature dependent with a coefficient of approximately 0.2% per °C [10]. In order to reduce this effect, there are two mechanisms available in TARGET 5. The ASIC is equipped with a continuous ring oscillator copy of the timebase generator (with one additional inverter) and its output is available for external monitoring and feedback control in firmware/software. The delayed copy of `SSTin` after the full chain of time delay elements, `SSTout`, is also available for monitoring and feedback.

Blocks of 32 storage cells are randomly accessible for readout from the storage array on demand. Once selected, the 32 storage cells in all 16 channels are powered up for Wilkinson ADCs. A Wilkinson ramp voltage generator block generates and broadcasts a ramp with adjustable duration and slew rate to all channels. The Wilkinson ramp slew rate is adjusted by varying the capacitor charging current, denoted `Isel`, or by changing an external ramping capacitor.

At a separately controllable start time, a 12-bit ripple counter (with adjustable speed) is begun for each channel. In order to support the fastest possible digitization, separate oscillators are provided for each counter. When the voltage ramp crosses the comparator threshold for a given sample voltage, the counter stops and the count then represents the time (ADC code) corresponding to the voltage held in the storage cell. In order to maintain a constant Wilkinson clock rate as a function of temperature, a separate, identical Wilkinson counter is provided inside the Wilkinson clock block for monitoring and feedback. Address decoding and sequencing is performed inside a serial readout sequencer block. Digitized values are randomly accessible for serial transfer on all 16 channels in parallel.

Digitization and readout can occur on demand, initiated by an external trigger signal. This external trigger signal can be generated by external logic based on the trigger primitives generated by TARGET 5 itself. Trigger primitives are formed based on the analog sum of four adjacent channels, referred to as a trigger group. Each ASIC provides four trigger primitives from four independent trigger groups. Furthermore, the contribution from each individual channel to the sum can be disabled in order to mask out noisy

[1] $\sim$\$35 per channel for the realization discussed in this paper, estimated $<$ \$20 per channel in a large production on the scale required for several dozen CTA telescopes.

[2] Within CTA, using a hardware coincidence trigger between telescopes is not planned for GCTs, but it is foreseen for SCTs.