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Drain current model for short-channel triple gate junctionless nanowire transistors

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ABSTRACT

This work proposes a numerical charge-based new model to describe the drain current for triple gate junctionless nanowire transistors (3G JNT). The drain current is obtained through a numerical integration of a single expression that physically describes the junctionless charge density in both accumulation and depletion regimes of operation, leading to a continuous model in all operational regions. The triple gate structure is modeled from an evolution of a previous model designed for double gate junctionless nanowire transistors (2G JNT). Improvements concerning the capacitance coupling, the internal potential changing while reducing the fin height in nanowire transistors and higher immunity to short-channel effects (SCE) are considered. The model validation is performed through both tridimensional numerical simulation and experimental measurements for long and short-channel devices. Through simulated results, it is verified the agreement of the modeled curves for junctionless transistors with different values of fin height. Comparison between the proposed model and experimental data is performed for 3G JNT advanced structures with channel length down to 15 nm and fin height of 8 nm. Results for 3G JNTs with different values of doping concentration and channel width are also displayed showing a good agreement as well. Moreover, 3G JNT performance is also analyzed and compared in the studied structures by extracting the threshold voltage (V_{TH}), subthreshold slope (S), *DIBL* and model parameters.

1. Introduction

Scientific community and microelectronic industry have massively invested in novelties to improve technology in order to continue the CMOS roadmap reducing the occurrence of SCE while scaling down the transistors dimensions [1].

One of the solutions for improving the electrostatics of sub-22 nm MOSFETs is the adoption of different tridimensional device structures known as multiple gate devices [1–5]. Their use allows the scaling of MOSFETs beyond the limits imposed by planar transistors [4,6,7]. These solutions can be combined with the use of different materials to improve the carrier mobility such as strained devices and Silicon-Germanium alloys [8–11].

The shortening of the channel length of the transistors requires accurate process to fabricate abrupt junctions between source-channel and drain-channel in inversion mode (IM) transistors. In order to overcome some problems on the fabrication process of nanoscale devices, a new structure called junctionless nanowire transistor (JNT) (Fig. 1) has been proposed [12,13]. The JNT is basically a uniformly doped stripe of silicon from source to drain terminals, surrounded by the gate stack, working as a multiple gated resistor [14]. The junctionless transistors seem to be an interesting proposal for the ultimate technological nodes, once it has shown many advantages over IM transistors for both analog and digital applications [15–17].

JNTs operate similar to accumulation mode transistors and have three regimes of operation: full depletion, partial depletion and accumulation. Doping concentration, gate material and silicon thickness must be well adjusted, such that with no gate to source voltage (V_{GS}) applied the channel region is fully depleted, there are no carriers flowing and the device is turned off. Considering an n-type JNT, when V_{GS} is higher than the threshold voltage (V_{TH}), the transistor works on partial depletion regime. As the depletion region reduces from the center of the silicon layer, a body current appears and the device is turned on. For V_{GS} higher than the flat-band voltage (V_{FB}), carriers accumulate at the surface, there is no longer depletion and a surface current starts to flow together with body current [12].

Recently, several models have been developed to describe the drain current (I_{DS}) of 2G JNTs (Fig. 1.a) [18–21] and a few for 3G JNTs [22,23]. The most part of JNT models in literature considers two expressions for the drain current and the transition between depletion and accumulation regimes is taken by using smoothing functions. Differently to these models, in this work, we present a new model to describe the drain current of 3G JNTs (Fig. 1.b and c), considering an unified

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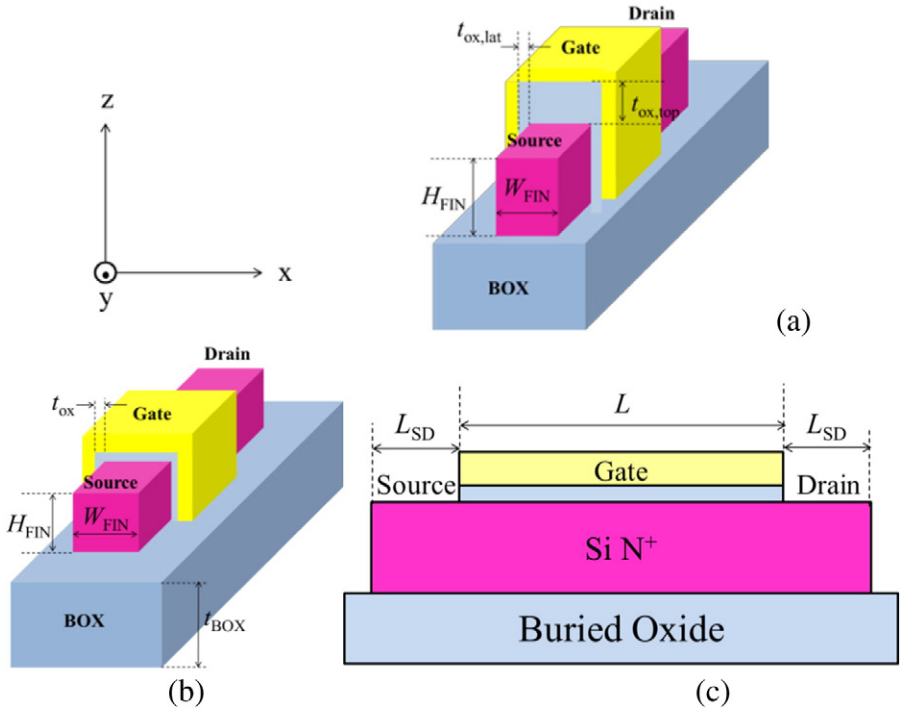

Fig. 1. Double gate junctionless nanowire transistor perspective (a), triple gate junctionless nanowire transistor perspective (b) and cross section (c).

expression to the charge density, leading to a single expression for the drain current continuous in all operation regimes.

The proposed model is based on a previous one first developed in [21] for long channel 2G JNT, with proper adjust in the device electrostatics to accomplish the effects of the top gate while moving to a 3G structure and then including short channel effects (SCE) [24]. The approach of correcting the electrostatics to adapt the 2G JNT model to describe 3G JNTs has been first presented in [25], where the expression for the drain current is presented only for long channel transistors. The model presented in this work has evolved from [25] accounting for the influence of changing any dimension associated at each of the three directions (x, y and z in Fig. 1), i. e. the model describes the drain current for junctionless transistors with different values of fin height (H_{FIN}), fin width (W_{FIN}) and channel length (L). This work presents all the expressions needed to describe short channel 3G JNTs in details, with the following effects comprised: velocity saturation, mobility degradation due to vertical and lateral electric field, channel modulation, threshold voltage roll-off, subthreshold slope degradation with channel length shortening, *DIBL*, series resistance, fringe capacitance influence and oxide charge density. The changing in the internal potential with the variation of H_{FIN} and L are also described. Moreover, fitting parameters and extracted electrical characteristics (V_{TH}, S and *DIBL*) are presented in this work, which are useful guidelines for device modeling and designs.

Model validation is performed with both three-dimensional numerical simulations and experimental measurements performed on SOI 3G JNTs fabricated at CEA – Leti [26] with channel width and gate length down to 7 nm and 15 nm, respectively.

2. Model description

The electric field expression is obtained from the charge density, considering a symmetric 2G JNT structure, where the potential variation occurs only through the axis related to the fin width. To express the 3G JNT behavior and include the silicon thickness influence on the intrinsic potential, a new expression to determine the surface potential is developed, which solution is obtained numerically. Then, the mobile charge is calculated as a function of the surface potential and integrated to give the drain current expression for long channel 3G JNT. The short channel effects are included at the end, by calculating the difference in the minimum potential between long and short channel transistors, the effective channel length and the effective mobility. The full description of the proposed model will be detailed in this section.

2.1. Long channel triple-gate junctionless nanowire transistor

Initially, it is considered that the potential varies only in the x direction. The charge density (ρ) as a function of the intrinsic potential (φ) and the potential drop between drain to source (V) in the semiconductor can be calculated according to Eq. (1) [27]. If only the potential associated to W_{FIN} direction is considered, the following expression will be able to describe a long channel 2G JNT, on the same way as the model proposed by Cerdeira et al. [21]. Both depletion and accumulation charges are comprised in this expression.

$$\rho = qN_D\left(-e^{\frac{\varphi - V}{\varphi_t}} + 1\right) \tag{1}$$

where q is the electron charge, N_D is the doping concentration and $\varphi_t = kT/q$ is the thermal potential at temperature T.

Applying one dimension Poisson's equation to the silicon layer from the surface interface to the center [21], the surface electric field is equal to

$$E_S = \text{sign}(\alpha)\sqrt{\frac{2qN_D\varphi_t}{\varepsilon_{Si}}}\sqrt{e^{\frac{\varphi_S - V}{\varphi_t}} - e^{\frac{\varphi_0 - V}{\varphi_t}} - \left(\frac{\varphi_S - \varphi_0}{\varphi_t}\right)} \tag{2}$$

where φ_S is the surface potential, ε_{Si} is the dielectric constant of the silicon, φ_0 is the potential at the center of the silicon layer and α is the difference of potential from surface to center, normalized by φ_t ($\alpha = (\varphi_S - \varphi_0)/\varphi_t$), expressed through the Lambert function by

$$\alpha = \alpha_{st} + LW\left[-\alpha_{st}e^{-\alpha_{st}}e^{\frac{\varphi_S - V}{\varphi_t}}\right] \tag{3}$$