Microelectronics Reliability 63 (2016) 42–45

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Resistive switching properties of a thin SiO_2 layer with CeO_x buffer layer on n^+ and p^+ Si bottom electrodes

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ARTICLE INFO

Article history:
Received 10 March 2016
Received in revised form 23 May 2016
Accepted 22 June 2016
Available online 1 July 2016

Keywords:
Resistive switching
Breakdown
Work function
Interface state density

ABSTRACT

Resistive switching properties of a 2-nm-thick SiO_2 with a CeO_x buffer layer on p^+ and n^+ Si bottom electrodes were characterized. The distribution of set voltage (V_{set}) with the p^+ Si bottom electrode devices reveals a Gaussian distribution centered in 4.5 V, which reflects a stochastic nature of the breakdown of the thin SiO_2. Capacitance–voltage (C–V) measurements indicate the trapping of electrons by positively shifting the C–V curve by 0.2 V during the first switching cycle. On the other hand, devices with the n^+ Si bottom electrodes showed a broad distribution in V_{set} with a mean value higher than that of p^+ Si bottom electrode devices by 0.9 V. Although no charge trapping was observed with n^+ Si bottom electrode devices, a degradation in interface states was confirmed, causing a tail in the lower side of the V_{set} distribution. Based on the above measurements, the difference in the V_{set} can be understood by the work function difference and the contribution of electron trapping.

1. Introduction

Resistive switching devices with a metal oxide resistive layer have attracted great interests as a fast operation at low voltage with excellent retention properties can be achieved [1,2]. The change in resistance between low resistance states (LRS) and high resistance state (HRS) has been modeled by a conductive filament formation in the resistive oxide layer, where both states are determined by the annihilation and the formation of the oxygen vacancies near one of the electrodes [3]. Materials used for electrodes have been reported to influence memory characteristics, including both memory types; unipolar and bipolar switching, and its switching characteristics [4]. For example, noble metals such as Pt, Au, and Ru, which are resistant to oxidation, show unipolar resistive switching characteristics, where Joule heat annihilates the tip of the filaments [2,5,6]. On the other hand, metals with strong oxygen affinity such as W or Ti exhibit bipolar switching behaviors, where oxygen atoms stored in the metal are extracted back to the filaments [2]. Indeed, both mechanisms have been numerically confirmed through simulations [7]. Also, work function of the electrodes is reported to shift the voltage needed to change the resistance state [8]. However, when a different metal is used, the difference in the chemical nature, including free energy to oxygen atoms, also changes the resistive switching characteristics. In addition, since most of the resistive switching devices consist of metal-insulator-metal (MIM) structures, charge trappings into the resistive layer may also change the properties, including set/reset voltages and retentions. Although it is important to understand those effects on the resistive characteristics, it is not easy to extract the causes separately from electrically measured data. To extract the effect of work function differences and the charge trappings on the resistive switching characteristics, it is straightforward to use semiconductor substrates with different dopings as electrodes; namely p^+ and n^+ Si, which possess work functions of 4.09 and 5.13 eV, respectively. By using the same materials as one of the electrodes, the chemical properties will be kept essentially the same. In this work, atomically flat single crystalline Si substrates were used as bottom electrodes so as to eliminate any structural effect due to roughness. The structure also reflects one-transistor one-resistance (1T1R) type memory cells assuming an integration of the resistive memory on source region of transistors. The resistive layer used in this work is thin SiO_2 layers with CeO_x buffer layers atop. The resistive switching behavior from HRS to LRS is understood based on the soft-breakdown of the thin SiO_2 layers under positive voltage to the top electrode by large contrasts in the dielectric constants (k) of these layers ($k_{SiO2} = 3.9$ and $k_{CeOx} = 28$). Since the bandgap of the CeO_x is small ($E_g = 2.4$ eV, depending on the stoichiometry) [9], the current will flow through the breakdown spots, achieving LRS [10]. The anodic oxidation of the breakdown spots with the use of a high oxygen ionic conductivity of CeO_x under negative bias to the top electrode will re-oxidize the breakdown spots, thus achieving HRS. Based on the two mechanisms, the cell exhibits the bipolar type switching behavior. The detailed switching mechanism is reported in ref [11].

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http://dx.doi.org/10.1016/j.microrel.2016.06.013
0026-2714/

2. Device fabrication and measurements

Devices were fabricated on (100)-oriented p^+ Si and n^+ Si single crystalline bottom electrodes with resistivity 0.002 Ω-cm and 0.001 Ω-cm, respectively. After chemical cleaning followed by a HF dipping process, a thermal dry oxidation process was carried out at 850 °C for 5 min to form a 2-nm-thick SiO_2 layer. Then, CeO_x films with a thickness of 5 nm were deposited on both samples by e-beam evaporation at 10^{-4} Pa with the oxygen gas flow of 0.4 sccm at a substrate temperature of 300 °C. The composition of the CeO_x layer was characterized by x-ray photoelectron spectroscopy, and was found to be $x = 1.6$ [12]. A 50-nm-thick W layer was deposited by sputtering on the CeO_x layers and patterned by reactive ion etching using SF_6 chemistry to form the top electrodes. After removing the SiO_2 layer on the backside of the wafer, an Al film with a thickness of 50 nm was thermally evaporated on the backside contact. The backside Al electrode was used as a terminal for bottom electrodes. Finally, the samples were annealed at 420 °C for 30 min in forming gas (H_2:N_2 = 3%:97%) ambient to terminate dangling bonds at SiO_2/Si interface. For electrical characterization, voltage ramping current measurements limited by current compliance (CC) were conducted by Agilent 4156C. For capacitance–voltage (C–V) measurements, Agilent E4980A LCR meter with a frequency of 100 kHz was used. An area of $20 \times 20\ \mu m^2$ for top electrodes was used to examine the resistive switching behaviors.

3. Resistive switching behavior with voltage sweeping

Both p^+ and n^+ Si bottom electrode samples showed bipolar-type resistive switching [9]. Irrespective of the initial forming process, the set processes were only observed when a positive bias was applied to the top electrodes and the reset process at negative bias to the top electrodes. This fact is one of the supporting evidences of the resistance change mechanism; breakdown and the anodic oxidation of the thin SiO_2 layer with the CeO_x buffer layer. Fig. 1 shows the typical resistive switching behavior for devices with p^+ and n^+ Si bottom electrodes for 100 times of switching operations including first forming process.

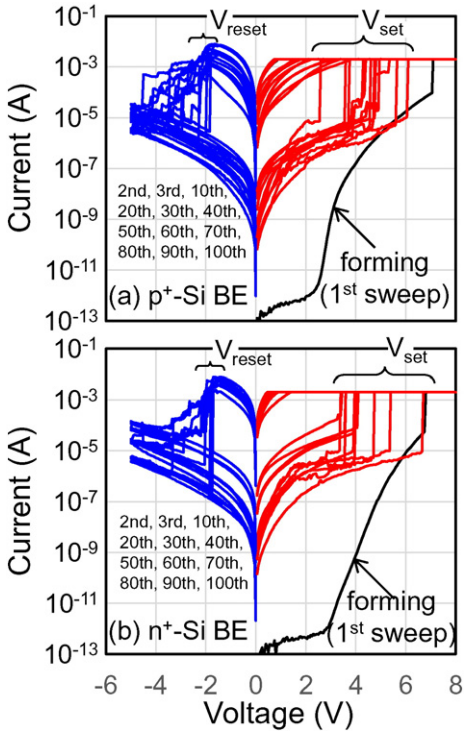

Fig. 1. Resistance change of W/CeO_x/SiO_2 on (a) p^+ Si and (b) n^+ Si bottom electrodes for the first 100 times. Also, the initial forming processes are shown.

In the set process, a voltage ramping up to 8 V and back to 0 V was applied to the W top electrode with a CC, and for the reset process, a voltage starting from 0 V down to −5 V and back to 0 V was applied without any CC. Jumps in current at positive voltage application correspond to set process to change the resistance state from HRS to LRS. A large scattering in the V_{set} can be observed for both bottom electrodes, which may be due to the stochastic nature of the breakdown spot for each voltage sweep [13]. The breakdown of SiO_2 films is known to have a correlation with positive charge trapping, where an enhancement in the electric field near the interface occurs [14]. Estimation of the amount of trapped charges will be discussed later by C–V measurements. On the other hand, the resistance of LRS is mainly determined by the value of the CC to avoid the catastrophic hard breakdown of the thin SiO_2. Here the current drops in the negative voltage sweeps indicate the change in the resistance state from LRS to HRS. The voltage needed for the reset process (V_{reset}) also showed large scattering, and several steps were needed to fully reset the resistance back to HRS.

The scattering of V_{set} is summarized in a histogram, shown in Fig. 2. The V_{set} of the sample with the p^+ Si bottom electrode follows a Gaussian distribution with a mean value and a standard deviation (σ) of 4.3 and 1.2 V, respectively, among switching cycles, indicating a random event for the breakdown. On the other hand, a tail in the distribution can be observed for the V_{set} obtained by the device with the n^+ Si bottom electrode. Also, a higher mean V_{set} value by 0.9 V than that of the devices with p^+ Si bottom electrode can be observed. The relationship between resistance (R_{off}) just before the jump in the current and the subsequent V_{set} is summarized in Fig. 3 for both devices with n^+ and p^+ Si bottom electrodes. From this figure, one cannot find any correlation between V_{set} and R_{off} including the forming process, suggesting that the condition of the re-oxidized spots do not affect the switching characteristics. This fact is in contrast to ionic metal oxides where a strong correlation is observed between V_{set} and R_{off}, which indicates that the gap length of the conductive filament affects the V_{set} [15,16].

To elucidate the contribution of charge trappings at or near the CeO_x/SiO_2 and the SiO_2/Si interfaces to the resistive switching characteristics, C–V measurements of both samples were conducted. Fig. 4 shows the C–V curves of the devices with p^+ and n^+ Si bottom electrodes of the first reset and after several reset processes under HRS. Note that the C–V curves at LRS could not be measured by the LCR meter due to large conductance through the switching devices, therefore, the top electrode voltage range for measurements was set below the V_{set}. For

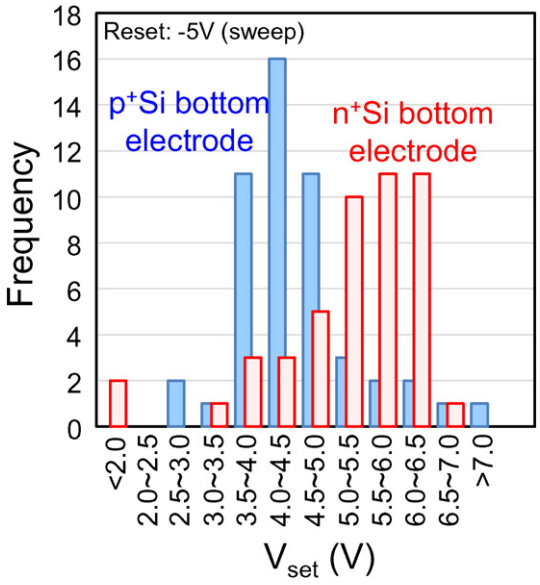

Fig. 2. Distribution of V_{set} obtained from voltage sweep to TE. Devices with the n^+ Si bottom electrode show higher mean V_{set} by 0.9 V.