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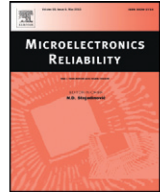

Thermal characterization of planar high temperature power module packages with sintered nanosilver interconnection

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ABSTRACT

Many new innovations have emerged in the power electronics industry to aid in meeting the expanded market demand. In spite of that the interest in high temperature and high power applications has fueled new developments in wide bandgap semiconductor devices which are capable of operation above 200 °C, silicon devices are still prevalent in the marketplace and offer significant power ratings at affordable prices. Researches have kept pushing the limit of the application temperature of silicon devices. The key to offering functional and reliable silicon packages that can endure higher temperatures is through innovative thermal management and packaging. Effective thermal management of packaged devices can be accomplished through materials selection, design or a combination of the two. In this paper, we outline a newly designed packaging structure and the fabrication process of a functional double-sided power module switching units utilizing LTJT sintered silver for each interface. The thermal characteristics of the power module were measured in various cooling scenarios utilizing thermal transient measurements, structure function analysis and the transient dual interface method (TDIM), techniques developed by Mentor Graphics. Significant improvement of thermal performance of the fabricated module was demonstrated. The resulting improvements in thermal resistance of the power module, thermal simulation model agreement and construction, and comparison of double sided thermal results to single sided conventions are discussed.

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1. Introduction

Currently, power module packages primarily consist of silicon devices, IGBTs and diodes, attached to an insulating substrate with soft solder alloys. Normally, the substrate is an insulating ceramic with eutectically bonded copper films attached to either side. These are called Direct Bond Copper (DBC) substrates and provide structural stability, electrical isolation and increased heat dissipation [1]. Available solder alloys utilized in these packages possess, on average, melting points below 250 °C. For electrically connecting the top terminals of these vertical devices to other circuit elements, arrays of aluminum or gold bonding wires are employed. Wires are bonded using various combinations of ultrasonic and\or thermal energy [2]. The wirebond connection density on the top surface is limited by the wirebond machine, technique and wire alloy. After wirebonding, the entire surface is coated with a flexible encapsulant. The encapsulant is meant only to reduce wirebond movement and protect device surfaces. All available encapsulation materials are relatively low in thermal conductivity with values <W/m K [3]. The contribution of the wirebonds and encapsulants to the overall heat dissipation of the module is negligible. Although advances have been made in the development of new substrates, die interconnection, encapsulants and the integration of each, most power modules are still constructed using this basic single sided attachment scheme. The move to increased temperature operation requires adoption of more thermally efficient designs and materials.

Changes in the conventional power electronics package which enhance thermal management may also serve to increase reliability. The components most often cited with the reduction in cycling lifetime are the wire bonds. Cyclic loading within the module result in wire-bond lift-off, increased flexural stresses in the wires, failure at each bonding site due to increased shear stresses and even work hardening of the aluminum wire [4]. Additionally, only utilizing wirebonds for top side electrical connections results in poor transient and steady state thermal performance [5]. Wirebonds have also been found to contribute to parasitic induction which translates directly into system losses and added heat [6]. Optimally, an area connection covering the entire top electrical pad would provide for uniform heat flux distribution from device self-heating and decreased parasitics [5]. With the addition of an increased thermal mass on the top of the device, both transient and steady state thermal characteristics can also be greatly enhanced [7].

Other secondary failures which lend to decreased reliability occur due to creep effects and crack propagation in the soldered die

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attachment [8]. These failure modes become more prominent as the operating temperature approaches that of the solder melting temperature. Lead-free solders are now the die-attach alloy of choice primarily because it is more environmentally friendly than previous solder alloys. However, even the melting temperatures of lead free solders are uncomfortably close to the expected operating temperatures of new device packages. Ideal die attach materials would possess melting temperatures significantly higher than the temperatures experienced in operation. This ratio is to as the homologous temperature ($T_{application}/T_{melting}$). It has been found that many solders which possess homologous temperatures (T_H) >0.8 (80% of the melting temperature) reveal increased joint degradation due to creep effects.

For these reasons, many new solder-free die-attach technologies have been examined to meet the demands for packaging high temperature devices. One promising technology, termed Low-Temperature-Joining-Technique (LTJT), was first introduced by Schwarzbauer nearly two decades ago [9]. Schwarzbauer's technique employed the use of silver particles which were sintered, rather than melted, at high temperatures and pressures resulting in a dense silver solid. Silver as an interconnect material has the advantage of having threefold higher thermal and electrical conductivity than solder attachments. And, because the melting temperature for silver is >960 °C, a sintered silver joint possesses a much lower homologous (<0.26) temperature than that of soldered joints.

Recently, several nanosilver paste formulations have been developed for eliminating or greatly reducing the pressure requirements (<5 MPa) during sintering [10–14]. The new nanoscale paste formulations take advantage of the increased surface energy of nanoscale particles to reduce the pressure requirements for both large and small die attachments. The LTJT technology is ideal for intricate packaging designs requiring multiple bonded interfaces. Because the sintered interface has a high melting point, it will not be affected by post-sintering thermal treatments. Unlike solder construction, multistep (3D) construction of sintered packages can be performed with the same nanosilver paste composition and will not result in degradation of previously sintered interfaces.

Others have proposed enhancing the package density through multilevel or embedded structures [15,16]. Yet, the optimum packaging solution for enhancing both the thermal characteristics and reliability of the conventional power module package is to create a symmetrical package utilizing heat sinks on both sides of the devices [17,18]. The increased thermal and electrical conductivity of silver LTJT provide an additional benefit. Three dimensional packages using a variety of die attachment methods have previously been proposed as a means to increase thermal management of the module and allow for function at higher application temperatures [19–23]. However, clear thermal resistance values and measurement methods of functional double sided packages have not been demonstrated.

In this paper we outline the fabrication of a double sided power electronics package designed for increased thermal management in high temperature applications. The package is thoroughly characterized using thermal transient measurements and structure function analysis with Mentor Graphics' T3Ster hardware and T3Ster Master and FloTHERM software tools. Because the structure benefits from double side cooling, multiple heat sinking configurations will be measured. And, lastly, the results of the measurements and the potential benefits for improved semiconductor cooling and simulation will be discussed.

2. Module design

Applications which stand to benefit the most from improvements in package reliability and thermal management are those that utilize high power conversion technologies. The most common power conversion architecture is a bridge network structure which utilizes three half bridge legs for converting DC power to three phase AC power and vice versa.

A half-bridge circuit is constructed from a high-side and low side switch with the output being drawn from the center of the two. The high side and low side configurations are identical which allows for further compartmentalization. The switching unit itself, which consists of one IGBT and antiparallel diode, is the lowest common denominator of the full topology. Fabrication of the smallest switching unit allows for the most flexibility in design and highest production yield.

The devices chosen for construction of one 1200 V, 150 A switching unit were an ABB IGBT model 5SMY 12M1280 and an ABB Diode model 5SLY 12J1200. The devices are both rated for a threshold voltage of 1200 V and a current of 150 A. Both the IGBT and diode are vertical devices having bottom contact dimensions of 13.5 mm × 13.5 mm and 10 mm × 10 mm, respectively. The diode thickness is 350 μm which is nearly double the IGBT thickness of 140 μm. The differences in device thickness are common and pose a large barrier to double-sided planar package fabrication.

The as-received emitter and anode surfaces require metallization, sometimes called Under-Bump-Metallurgy (UBM), to make the surface compatible with sintered silver and/or solders. The metallization was done using Pulsed Vapor Deposition (PVD). The PVD was used to apply 150 nm of Cr for adhesion to the AlSi layer, another 200 nm of Ni for a diffusion barrier and finally 250 nm of Ag for insuring a good bond to the sintered silver die attachment.

The substrate chosen for this project was a Direct Bond Copper (DBC) substrate with Al_2O_3 isolation ceramic purchased from Rogers/Curamik. The thermal conductivity of the substrate is referenced as 24–28 W/m K. The copper thickness is 0.3 mm and the isolation ceramic of alumina is 0.62 mm. The substrate was also provided with silver plating on both top and bottom copper surfaces for compatibility with LTJT processing. The bulk of the substrate is used as a trace width which will minimize parasitic inductance and reduce curvature stresses which occur when large amounts of metal are removed preferentially from one side of the substrate [19].

Ideally, for this configuration, the best electrical and thermal performance would be achieved by reduction of the spacing between top and bottom substrates. However, the top side spacing needs to be adjusted for various reasons the most important being the reduction in thermo mechanical stresses which arise during the fabrication steps. During fabrication, the paste will sinter at platen temperatures between 250 °C and 290 °C, depending on tooling mass. Thermo mechanical stresses accumulate as the entire assembly is cooled to room temperature. These stresses in a double sided package are likely to exceed the shear stress of the silicon device [24,25].

A design solution was sought that would address the shear strength by expanding the interface. The increase in joint thickness and compliance has been found to reduce thermo mechanical device stresses significantly [26]. Additionally, an adjustable joint may simplify the accommodation of device height differences. And, as an added benefit, the opening proves ideal for breakdown testing without encapsulation and post-fabrication encapsulation penetration. The compliant layer is fabricated from silver and added to the top substrate during the fabrication process and will thus result in an asymmetrical structure function for thermal analysis.

3. Module fabrication

Substrates were first patterned and etched. The bottom and top substrate are nearly identical with maximum dimensions of 25.4 mm by 45.8 mm. The bottom substrate provides the outside connection for the gate and emitter driver so it contains two added digits which will provide connections to outside gate drivers. The remainder of the bottom pad is solid and will provide parallel connection to the cathode of the diode and collector of the IGBT. The positive DC bus will be connected to the bottom substrate and commute to the top substrate through the devices. A schematic of the components and placement is shown in Fig. 1.

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