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# Protrusion of electroplated copper filled in through silicon vias during annealing process

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ABSTRACT

To investigate the protrusion behavior of the copper filled in through silicon via (TSV), four sets of TSV copper samples are prepared by using four level sets of electroplating current density and additive concentration, and then the samples are annealed with three temperature ramp rates, 10 °C/min, 1.2 °C/min and 0.6 °C/min, respectively. Protrusion of the copper in all of the samples after annealing is measured, and the grain size of the copper before and after annealing is examined. A mechanism of grain size evolution is developed to explain the protrusion process during annealing. A finite element (FE) model is also built up and a grain size dependent material model is introduced to explain the effects of electroplating parameter and annealing temperature ramp rate. Experimental and numerical results show that the sample filled by higher electroplating current density and higher additive concentration has smaller copper grain size both before and after annealing, and also has less protrusion. The protrusion strongly depends on the grain size both before and after annealing. The annealing temperature ramp rate has significant impact on the grain size and protrusion after annealing. The temperature ramp rate affects the protrusion by influencing grain size evolution process, and the mechanism is also validated by FE analysis. After all, an optimized annealing temperature profile is proposed to minimize the copper protrusion by restraining the growth of grain during annealing.



## 1. Introduction

Through-silicon-via (TSV) is one of the important technologies used in three dimensional microelectronics packaging [1,2]. With shortened interconnection length between multiple stacked conventional components (packages), TSV technology can improve the products with higher electrical performance, higher density, and lighter weight. There are six key steps to fabricate TSVs on a wafer [3–5], namely, silicon vias formed by deep reactive ion etching (DRIE), dielectric layer deposited on via wall by plasma enhanced chemical vapor deposition (PECVD), barrier and seed layers deposited by physical vapor deposition (PVD), copper filled in the vias by electroplating, and overburden copper removal by chemical mechanical polishing (CMP). After that, the TSV wafer is commonly annealed to stabilize the microstructure, increase ductility, relief internal stresses, and to decrease electrical resistance of the filled TSV copper. A typical TSV has a diameter of 5–50 μm with depth of 50–150 μm, and the depth-to-width ratio is in the range of 5–10.

In the TSV structure, large mismatch in the coefficient of thermal expansion (CTE) between the copper and its surrounding silicon matrix is critical to the TSV's reliability. CTE mismatch leads to great stress and deformation in the filled copper under thermal loadings. An important feature of the deformation is that the filled copper protrudes out of the silicon surface after annealing process or thermal cycling [6]. The kind of protrusion, on the one hand, could break the back-end of line (BEOL) layers during assemble process or in service [7,8]. On the other hand, the protrusion might cause delamination or cracking of the side wall interface between the copper and the dielectric materials [9,10]. Therefore, understanding of the protrusion behavior and its mechanism is important to the TSV reliability design and fabricating process optimization.

Wu et al. [11] use two different processing conditions to fabricate two types of TSVs with different grain sizes, and found that the TSV sample with smaller copper grain size protrudes less after annealing, in addition, the yield strength is also higher. They suggest that the fabricated TSVs with smaller copper grain size or higher yield strength would be helpful to reduce the protrusion. In fact, the grain size of the filled copper is affected by the electroplating parameters such as the bath chemistry concentration [12,13] and current density [14–16]. However, few investigations are conducted on the relationship among the electroplating parameters, grain size and protrusion of the filled copper, thus optimizing of the electroplating parameters is not well applied to control the copper protrusion.

The microstructure of TSV copper before and after annealing with increasing peak temperature has been examined experimentally [17–19], the results show that the higher annealing temperature produces

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**Table 1**
Test samples prepared by different electroplating parameters.

| Level set | Current density | Additive concentration [a)] |
|---|---|---|
| HH | 1.5ASD[b)] | 15 mL/L |
| HL | 1.5ASD | 10 mL/L |
| LH | 1.0ASD | 15 mL/L |
| LL | 1.0ASD | 10 mL/L |

[a] The additive is a kind of polymer materials.
[b] Average current density (ASD) = amperage power (Amp)/plating area ($dm^2$).

greater protrusion, and larger grains are also observed after annealing. It implies that the sample with larger copper grain size has a greater protrusion. Jiang et al. [20] explain this phenomenon as that the grain growth during annealing leads to greater grain size, and thus leads to lower yield strength of the copper due to the Hall–Petch effect, therefore it brought on larger plastic deformation and protrusion of the copper. However, Che et al. [17] and Heryanto et al. [18] point out that higher annealing temperature produces higher copper expansion and stress, and these consequentially result in greater protrusion, no matter whether the grain grows or not. They believe there is no evidence that the grain growth makes any direct contribution to copper protrusion. The contradictory explanations, which based on limited experimental observations, cannot provide us a clear picture about how the protrusion mechanism during the annealing. More elaborated experimental and theoretical study needs to be conducted.

Factors impacting the grain size of the filled copper in TSV samples are electroplating parameters, the peak annealing temperature and annealing time. Besides, the grain size evolution is not only dependent on the peak annealing temperature but also related to the temperature ramp rate used in the annealing process. To reveal and understand the effect of grain size evolution on the protrusion clearly, a fixed annealing peak temperature and three temperature ramp rates are used in this investigation.

To investigate the effects of electroplating parameter and annealing temperature ramp rate on the protrusion, four sets of samples are prepared by using four level sets of electroplating current density and additive concentration, and then the samples are annealed to a peak temperature 425 °C with three temperature ramp rates, 10 °C/min, 1.2 °C/min and 0.6 °C/min, respectively. The protrusion and the grain size of the copper before and after the annealing are measured. To interpret the protrusion behavior, a finite element model is built to predict the protrusion and a grain size dependent material model is applied to take into account the effects of electroplating parameter and annealing temperature ramp rate.

## 2. Experimental procedures

### 2.1. Test samples

The test samples were fabricated on a 100 mm wafer. The TSV diameter, depth and pitch were 30 μm, 100 μm and 200 μm, respectively. An insulating layer ($SiO_2$) was deposited to the via sidewall, then a barrier layer (TiW) and a copper seed layer sequentially. To study the effects of current density and additive concentration on the protrusion of samples, two levels of current densities and two levels of additive concentrations were selected to electroplate copper into the silicon via, and totally four sets of samples were received, as listed in Table 1. The four sets of samples were named HH (high current density and high additive concentration), HL (high current density and low additive concentration), LH (low current density and high additive concentration), and LL (low current density and low additive concentration). After the plating filled, a standard CMP process was employed to remove the residual overburden copper on the wafer surface, so that the copper would be able to protrude freely during the following annealing. During the sample preparing procedures, the emery paper of 0.25 μm grit size were used to obtain a more flat planer surface. Optical microscope was used to help acquiring a smooth polished surface. To remove the surface residual chemicals produced in the polishing process, the samples were cleaned using ultrasonic equipment with acetone.

A vacuum annealing furnace with Argon gas ambient was used to conduct the annealing process, in which the temperature was ramped up from 25 °C to 425 °C by a constant rate, and then hold for 30 min at the peak temperature. To investigate the effect of the ramp

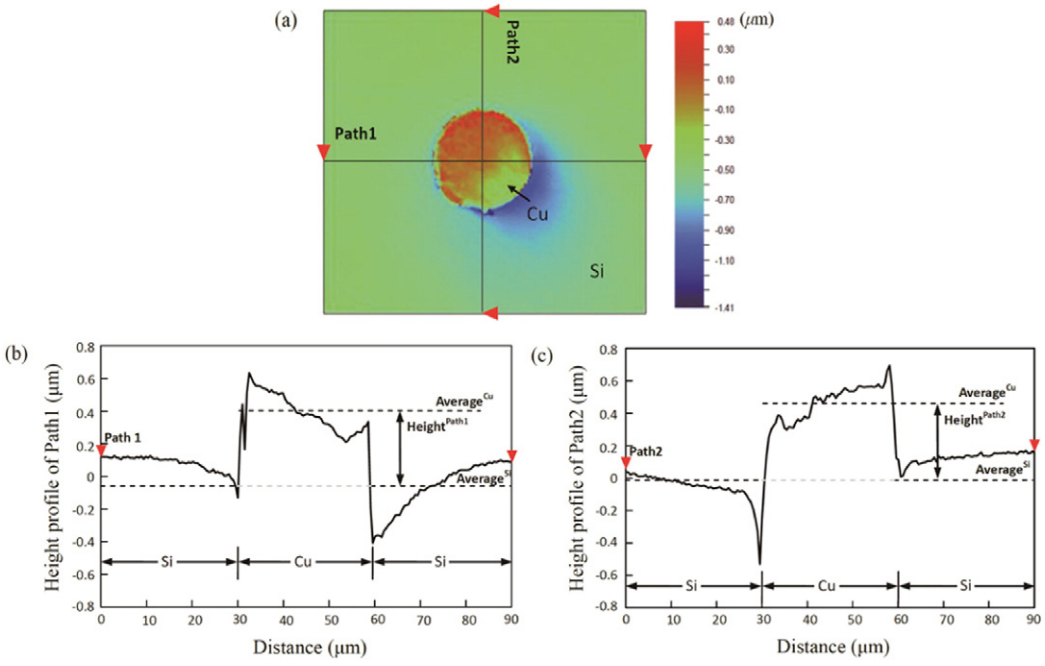


**Fig. 1.** Measurement procedure of protrusion: (a) 3D contour map of the sample surface, (b) height profile along Path 1, and (c) height profile along Path 2.