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Modeling and analysis of crosstalk induced overshoot/undershoot effects in multilayer graphene nanoribbon interconnects and its impact on gate oxide reliability

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ABSTRACT

Crosstalk induced overshoot/undershoot effects in multilayer graphene nano ribbon interconnects (MLGNRs) are investigated with the help of ABCD parameter matrix approach for intermediate level interconnects at both 11 nm and 8 nm technology node. The worst case crosstalk induced peak overshoot voltage for perfectly specular, doped multilayer zigzag GNR interconnects is comparable to that of copper interconnects. The performance of neutral GNR interconnects is better than that of its doped counterpart with respect to peak crosstalk overshoot. But from the perspective of overall overshoot width and overshoot area contribution, perfectly specular, doped MLGNR interconnects outperform all other alternatives. As far as the effective electric field across the gate oxide is concerned, the doped MLGNR interconnects outperform neutral ones and copper interconnects for all the cases. It is estimated that the doped perfectly specular multilayer GNR interconnects have gate oxide failure rates (*AFR*) of ~240× and ~790× lesser than copper interconnects for 11 nm and 8 nm technology node respectively. So, from the gate oxide reliability perspective, perfectly specular, doped multilayer zigzag GNR interconnects are great advantageous to copper interconnects for the future integrated circuit technology generations.
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1. Introduction

Interconnects play a major role in the system performance and reliability of future generation integrated circuits. According to ITRS-2013 roadmap [1], wire width and current density of Cu based interconnects are expected to reach 8 nm and 4.91×10^6 A/cm^2 respectively in the year 2027. Also, resistivity of Cu wire (i.e., expected to reach 10.81 μΩ-cm in the year 2027) increases with miniaturization of feature sizes due to interface and grain boundary scattering [2]. So, increased Joule heating (i.e., due to high resistance of the copper wire) leads to reduction of electro-migration lifetime and in turn overall current carrying capacity [3,4] is severely impacted. These bottlenecks of conventional Cu based interconnects demand some innovative solutions to overcome the critical challenges in performance, scaling, and reliability for future-generation on-chip interconnects.

Because of their exceptional electrical performance, 1D and 2D carbon nanostructures (i.e., carbon nanotube, graphene nanoribbon) have been considered as a potential alternative solution to Cu based interconnects. A comparison of the various properties of several interconnect materials is shown in Table 1.

Theoretically it has been shown that graphene has excellent transport properties, thermal conductivity, mechanical robustness [5–7], lower resistivity, higher maximum current density, and lower capacitance compared to copper in nanoscale dimensions [8]. Moreover, graphene is also advantageous because of its simpler fabrication processes, better material control and reproducibility, compared to multi-walled carbon nanotubes (MWCNT), a 1D carbon based nanostructure and a potential alternative interconnect material. Graphene-based interconnects could be used under various scenarios, such as carbon/metal hybrid interconnects, direct interface to graphene-based devices (switch, RF, memory, NEMS, etc.), and local level interconnects with huge demands in wire width scaling, current-carrying density, or cross-talk tolerance. Recently, graphene interconnect has been integrated with CMOS ring oscillator with an operating frequency of 1.3 GHz [9].

The compact physics based circuit model is developed for armchair and zigzag GNR interconnects in [10,11]. The performance of various

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[1] This is the specimen author footnote.
[2] Another author footnote, but a little more.

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Table 1
Various properties of the key interconnect materials.

Properties	Cu	W	SWCNT	MWCNT	Graphene
Max. current density (in A/cm2)	10^7	10^8	10^9	10^9	10^9
Thermal conductivity (in 10^3 W/m-K)	0.385	0.173	1.75–5.8	3.0	3–5
Melting point (in K)	1356	3695	3800	3800	3800
Mean free path at room temperature (in nm)	40	33	10^3	2.5×10^4	10^3
Temperature coeff. of resistance (10^{-3}/K)	4.0	4.5	1.1	−1.37	−1.47

types of GNR interconnects i.e., neutral, intercalation doped has been studied in [12]. The impact of various model parameters (i.e., bandgap, mean free path, Fermi level, and edge specularity) on the conductance and the delay is discussed comprehensively in this work. A stability analysis for GNR interconnect is performed in [13]. In this work, the dependence of the degree of relative stability for multilayer GNR (*MLGNR*) interconnects on the geometry of each nanoribbon has been studied. In [14], Das and Rahaman have performed crosstalk analysis in GNR interconnects and its impact on gate oxide reliability. Recently Crosstalk induced effects (i.e., delay and noise) are analyzed in multilayer GNR interconnects in [15–17]. In all these works, transient responses of the signals are analyzed using equivalent single-conductor (*ESC*) model at 22 nm and 14 nm technology nodes.

In all the above mentioned methods, the crosstalk induced effects are analyzed using SPICE simulations. However, to ensure circuit performance and reliability, interconnect analysis must be considered at the early phases of the design cycle. On-chip interconnects can be analyzed based on either simulation techniques or closed-form analytic formulas. Simulation tools like SPICE use numerical integration or convolution techniques for producing very accurate results. However, these techniques are computationally expensive to be used at the full-chip level [18]. Therefore, a non-SPICE based model is necessary to develop for analyzing crosstalk induced effects in the high density, high speed chips. The ABCD parameter matrix based model has been proposed for analyzing crosstalk induced delay and noise in SWCNT bundle interconnects [19], MWCNT bundle interconnects [20,21] and multilayer GNR interconnects [22].

1.1. Contributions of the paper

The novel contributions of the work are summarized below:

- In this work, ABCD parameter matrix based model is utilized to analyze crosstalk induced overshoot/undershoot effects in multilayer neutral and doped zigzag GNR interconnects of various specularity at both 11 nm and 8 nm technology node.
- From the estimated overshoot/undershoot voltage, gate oxide reliability is analyzed. It is found that doped perfectly specular multilayer GNR interconnects have gate oxide failure rates (AFR) of ~240× and ~790× lesser than copper interconnects for 11 nm and 8 nm technology node respectively.

The rest of the paper is organized as follows. Section 2 presents the electrical model for both copper and graphene based interconnects. Section 3 briefly discusses the crosstalk induced overshoot/undershoot effects. Section 4 explains the gate oxide reliability. Section 5 focusses on results. Finally the conclusions are drawn in Section 6.

2. Electrical equivalent model

2.1. Equivalent electrical parameters of copper interconnect

Fig. 1 shows a conventional copper interconnect system. In the figure shown, parameters r_p, l_p, C_{gp} and C_{cp} denote per unit length (p.u.l) resistance, self-inductance, electrostatic ground capacitance and electrostatic coupling capacitance between adjacent wires respectively. Inverting buffers are used to implement the driver and load is capacitive, denoted by C_i (i.e., it basically corresponds to the input capacitance of the load inverting buffer). Here, buffers are modeled as an equivalent RC circuit with a high degree of accuracy [23]. The parameters of the buffers are R_d, C_o and C_i. R_d, C_o and C_i are the equivalent switching resistance, equivalent diffusion capacitance and equivalent gate capacitance of a minimum sized inverter buffer. The RC parameters (i.e., R_d, C_o and C_i for the driver/load buffer for various technology nodes are shown in Table 2. The technology parameters for various levels of copper interconnects are obtained from ITRS-2013 roadmap and shown in Table 3 [1]. The analytical equations used to calculate distributed RLC parameters (i.e., r_p, l_p, C_{gp} and C_{cp}) of copper interconnect are shown below in Eq. (1)–(4) [24]. RLC parameters of the copper interconnect are shown in Tables 4 and 5.

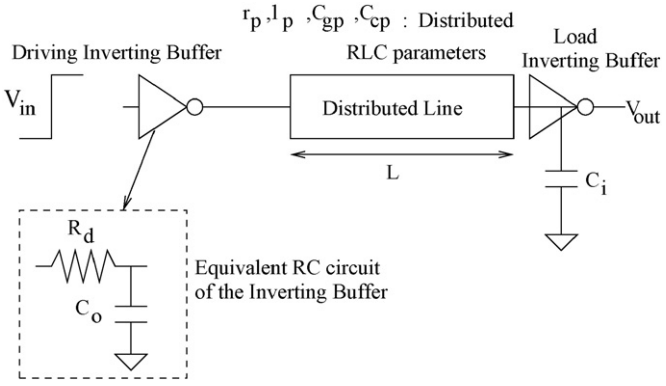

Fig. 1. Electrical equivalent model of a typical copper interconnect system.

$$r_p = \frac{\rho}{w \cdot t} \tag{1}$$

$$l_p = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{2L}{\omega + t}\right) + \frac{1}{2} + \frac{0.22(\omega + t)}{L}\right] \tag{2}$$

$$C_{gp} = \varepsilon_0\varepsilon_r\left[\frac{\omega}{ht} + 2.22\left(\frac{s}{s + 0.70ht}\right)^{3.19} + 1.17\left(\frac{s}{s + 1.51ht}\right)^{0.76}\left(\frac{t}{t + 4.53ht}\right)^{0.12}\right] \tag{3}$$

$$C_{cp} = \varepsilon_0\varepsilon_r\left[1.14\frac{t}{s}\left(\frac{ht}{ht + 2.06s}\right)^{0.09} + 0.74\left(\frac{\omega}{\omega + 1.59s}\right)^{1.14} + 1.16\left(\frac{\omega}{\omega + 1.87s}\right)^{0.16}\left(\frac{ht}{ht + 0.98s}\right)^{1.18}\right] \tag{4}$$

where, L is length, w is width, t is thickness, ρ is resistivity, ht is height of the interconnect above ground plane, s is spacing between adjacent interconnects, ε_r is dielectric constant, ε_0 is permittivity in the free space and μ_0 is permeability in the free space.

2.2. Electrical modeling of multilayer GNR interconnects

In graphene, the carbon atoms are arranged in a honeycomb structure. Depending on the orientation of carbon atoms, the edge of the graphene sheet is either armchair or zigzag. Zigzag GNR (i.e., zz-GNR) is always metallic whereas armchair GNR can be either semiconducting or metallic depending upon geometry (chirality). For interconnect

Table 2
RC parameters of the inverting buffer for various technology nodes.

Parameters	11 nm	8 nm
R_d (in KΩ)	42.1	65.8
C_o (in fF)	0.012	0.007
C_i (in fF)	0.036	0.021

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