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High-resolution wide-band *LC*-VCO for reliable operation in phase-locked loops☆

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ABSTRACT

This paper presents a novel sizing scheme to implement the array of switches in the capacitor bank of *LC*-VCOs for oscillation frequency coarse control. The proposed scheme allows increasing the number of elements in the capacitor bank beyond the values typically achieved by binary scaling, endowing the resulting *LC*-VCO with a wider tuning range and high frequency resolution, which is beneficial for the implementation of reliable phase-locked loops. Two different gigahertz *LC*-VCOs have been designed to validate the proposed scheme. The prototypes, fabricated in a cost-effective 0.18 μm CMOS process, cover a 700 MHz frequency range from 1.35 GHz to 2.05 GHz and from 2.05 GHz to 2.75 GHz, respectively, with a phase noise figure of −122 dBc/Hz and −119.5 dBc/Hz at 1 MHz from the mid-range carriers, and a power consumption of 18 mW. These figures result in a respective FOM_T of −186.4 dBc/Hz and −183.8 dBc/Hz. The performance of the fabricated *LC*-VCOs is achieved in each case with a dense coarse tuning range of 128 levels, which allows, respectively, a fine tuning gain smaller than 40 MHz V^{-1}.

1. Introduction

Phase-locked loops (PLLs) are a basic building block in a great number of applications. Its operation achieves the synchronization of an oscillator embedded in the integrated circuit (IC) with a very stable external timing reference, typically a crystal oscillator, and for this reason the control voltage of a PLL carries very precise information about the effect of process, voltage and temperature (PVT) variations in the operation of the IC. In this respect, there is an increasing interest in the deployment of integrated PLLs along with both digital and RF circuits to provide information about the effect of PVT variations to correct it, thus increasing the robustness and reliability of the system. For instance, in [1] an on-chip PLL is used to generate the adaptive body bias in an RF power amplifier, minimizing the effect of PVT variations on its performance. A key parameter to evaluate the performance of PLLs, and therefore their suitability for sensing applications, is its phase noise.

The phase noise of PLLs is strongly related to the phase noise of the voltage-controlled oscillator (VCO) in the PLL. For this reason, resonant *LC*-VCOs are preferred over ring VCOs for the design of PLLs due to their better phase noise performance. Nevertheless, the phase noise of a PLL also shows a tight dependency on the frequency tuning gain of the oscillator (K_{VCO}) [2]. In particular, as K_{VCO} increases, any ripple present at the control voltage of the VCO translates to greater frequency variations on its output signal and thus to and increase of the phase noise of the PLL, which has a negative effect on its performance and reliability.

The frequency tuning of an *LC*-VCO is carried out modifying the capacitance of an MOS varactor, whose variation is around 10% of its nominal value. Because the oscillation frequency of an *LC*-VCO is given by $f_{osc} = \frac{1}{\sqrt{LC}}$, where *L* and *C* are, respectively, the equivalent inductance and capacitance of the resonant *LC*-tank, the 10% variation in *C* translates into a 5% variation in f_{osc}, which is not wide enough to guarantee reliable operation under process, voltage and temperature (PVT) variations, and therefore demands the implementation of specific techniques to increase it. On the other hand, achieving a wide continuous frequency variation is not desirable either because it would magnify the ripple in the control voltage, resulting in an increase in phase noise and therefore in higher output jitter.

For these reasons, the most commonly used technique to widen the frequency range of *LC*-VCOs consists in adding a set of switched capacitors in parallel to the MOS varactor (Fig. 1a). If the capacitance of the elements in the switched capacitor bank are scaled in powers of 2, their contribution of the total *LC*-tank capacitance is linearly modified by a digital word whose bits control whether the elements in the bank are connected or disconnected from the *LC*-tank. In this structure, therefore, the varactor provides the continuous fine tuning of the *LC*-VCO whereas the switched capacitor bank provides its coarse tuning with finite frequency steps.

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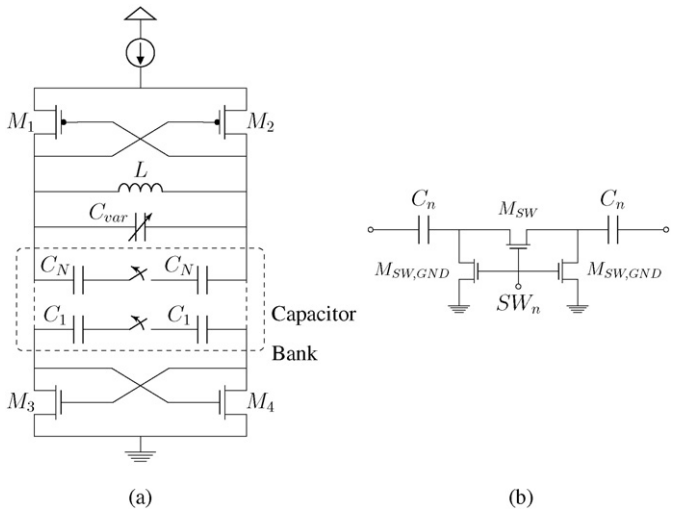

Fig. 1. (a) Schematics of an *LC*-VCO, with negative transconductance (M_1–M_4), inductor (L), varactor (C_{var}), and switched capacitor bank ($C_1 \ldots C_N$). (b) Schematics of NMOS switch with π configuration.

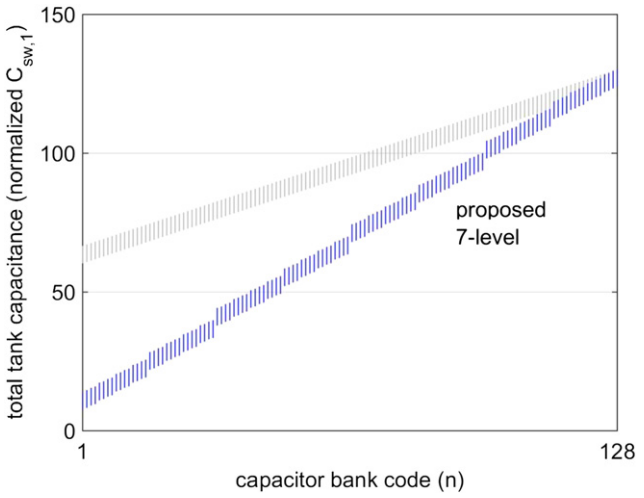

Fig. 3. Representation of the combined coarse and fine capacitance of a 7-level bank with switches scaled according to the proposed scheme in comparison to traditional binary scaling. The all-OFF capacitance (capacitor bank code $n = 1$) coincides with the ideal value and the dependence is practically linear.

Ideally, the elements of the switched capacitor bank should contribute their nominal capacitance when connected to the *LC*-tank and a zero capacitance when disconnected. Consequently, if the capacitances are binary scaled, their contribution varies linearly from zero to a maximum value according to the digital control word and therefore the frequency range of the resulting *LC*-VCO can be extended, doubling it to any desired value, just by adding new binary-scaled capacitors. This is relevant because adding more coarse bands to the frequency tuning range of the oscillator alleviates the fine gain requirements for each band, which improves the reliability of the PLL.

Real *LC*-VCOs use NMOS switches to connect the capacitors to the *LC*-tank. To decrease their parasitic resistance and not degrade the Q factor for better phase noise, switch transistors are doubled in size following the tank capacitors. Nevertheless, this has a negative effect in that their OFF parasitic capacitance also increases, thus reducing the overall tuning range. This is analyzed in [3], where it is concluded that increasing the size of the switched capacitor bank beyond 6 elements has no beneficial effect on the tuning of *LC*-VCOs. According to this result, thus, the number of coarse bands in *LC*-VCOs is limited to 64, which in turn has an effect on the minimum fine tuning gain achievable and therefore on the operation reliability of the PLL.

Preliminary simulation results reported in [4] showed that acting on the sizing of the transistors in the switches allows overcoming the limit of 6 elements established in [3], therefore achieving increased frequency resolution over a wide tuning range. In particular, [4] shows that increasing the size of the transistors acting as switches in the *LC*-tank in binary steps results in a narrow capacitance variation for large *LC*-tanks, whereas a significant increase in the capacitance variation, almost equalling the value expected for ideal parasitic-less switches, with an almost linear capacitance characteristic can be achieved stepping the size increments into fewer levels.

This paper demonstrates experimentally the proposed scheme by two *LC*-VCOs incorporating a 7-element capacitor bank. The prototypes are fabricated in a reliable and cost-effective 0.18 μm CMOS process, whose feasibility to implement reliable, low-power multi-gigahertz oscillators has already been shown [5]. One of the *LC*-VCOs (VCO 1) covers a wide 41% tuning range from 1.35 GHz to 2.05 GHz in 128 overlapping bands, allowing a fine tuning gain lower than 40 MHz V^{-1}. The other one (VCO 2) incorporates the same capacitor bank, thus achieving the same 700 MHz tuning range, from 2.05 GHz to 2.75 GHz, also in 128

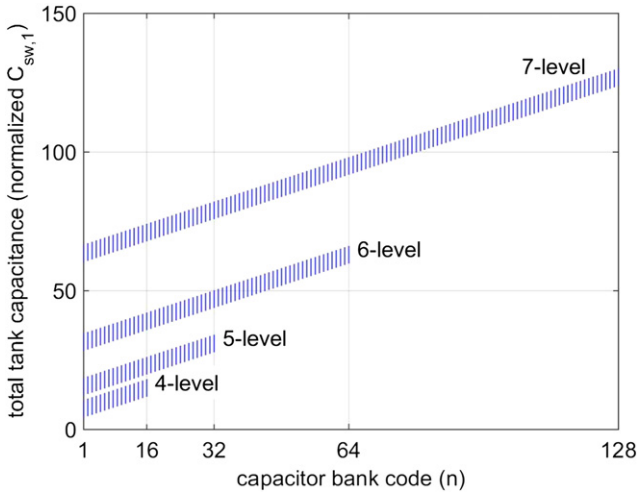

Fig. 2. Representation of the combined coarse and fine capacitance of 4-level to 7-level banks with binary-scaled switches. As a new element is added to the bank, the parasitic capacitance of its switch increases the all-OFF bank capacitance (capacitor bank code $n = 1$), reducing the tuning range.

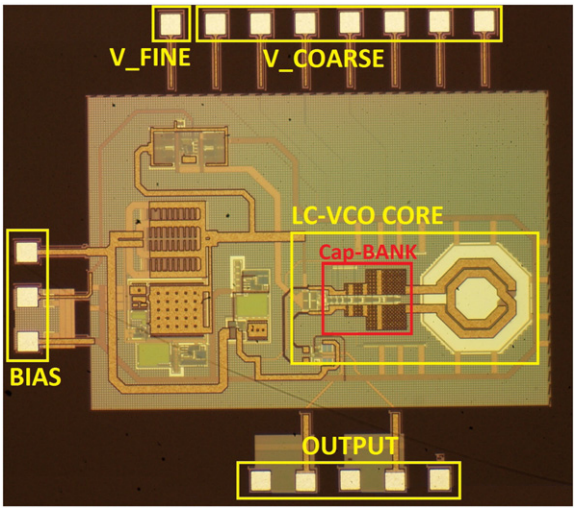

Fig. 4. Micro-photograph of the fabricated 2.05 GHz to 2.75 GHz *LC*-VCO (VCO 2). Dimensions 780 μm × 430 μm.