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A new high dynamic range ROIC with smart light intensity control unit

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ABSTRACT

This journal presents a new high dynamic range ROIC with smart pixel which consists of two pre-amplifiers that are controlled by a circuit inside the pixel. Each pixel automatically decides which pre-amplifier is used according to the incoming illumination level. Instead of using single pre-amplifier, two input pre-amplifiers, which are optimized for different signal levels, are placed inside each pixel. The smart circuit mechanism, which decides the best input circuit according to the incoming light level, is also designed for each pixel. In short, an individual pixel has the ability to select the best input amplifier circuit that performs the best/highest SNR for the incoming signal level. A 32 × 32 ROIC prototype chip is designed to demonstrate the concept in 0.18 μm CMOS technology. The prototype is optimized for NIR and SWIR bands. Instead of a detector, process variation optimized current sources are placed inside the ROIC. The chip achieves minimum 8.6 e^- input referred noise and 98.9 dB dynamic range. It has the highest dynamic range in the literature in terms of analog ROICs for SWIR band. It is operating in room temperature and power consumption is 2.8 μW per pixel.

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1. Introduction

Today's modern focal plane arrays (FPA) are recent technologies. The first generation FPAs are only single-dimensional linear structures developed in the 1950s. Those FPAs are used with scanners to generate two-dimensional images. The second generation FPAs are hybridized with two-dimensional staring detectors in the 1970s. Right now, we are in the era of the third generation systems. They promise more on-chip functionality, capability, and performance for pixels such as analog to digital conversion inside a pixel instead of column level, very large number of pixels (2048 × 2048), usage of dual or multi-color detectors, some pre-processing functionalities within a pixel and utilization of cheap uncooled technologies [1].

New ROICs have been developed over the last decade to meet the performance requirements of the third generation FPAs. Digital integrated readout of circuits (DROICs) are one of them. They promise very large charge handling capacities such as 1—3Ge^-, high SNR values with high-resolution conversion capabilities and very low power [2–4]. There are some drawbacks associated with DROICs such as high cost due to the usage of advanced technology node. Moreover, DROICs are mostly suitable for LWIR and MWIR due to high current levels and not so great power consumption levels with considerably large pixel area requirements.

Another approach is developing smart ROICs that includes on-chip processing capabilities and functionalities to reduce processing overhead or improve performance [5–7]. Due to the functionalities added into pixel structure, pitch sizes of these ROICs are bigger than trending small pitch sizes. So these ROICs aim low spatial resolution applications.

Another popular trend for the third generation FPAs is dual or multi-color imaging systems [8–10]. These systems have either one or two connections to input cells and input cells have multiple input amplifiers that are each optimized for a detection band to achieve the best performance.

Typical unit cell of a ROIC consists of input amplifier, gain switches, multiplexer, output amplifier, and some control switches. For a standard single band detector array a ROIC uses only single input amplifier which is optimized for average performance. Moreover, gain switches inside unit cell used to adjust capacitance value at the integration node which allows to change charge handling capacity. In other words, increasing integration capacitance allows to handle larger signals while compromising noise performance.

In this work, the design of readout integrated circuits (ROIC) for infrared focal plane arrays (FPAs) with high dynamic range (HDR), utilizing a smart input circuit selection mechanism is presented. HDR for ROIC corresponds to very dark and bright signal levels

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being processed at the same time, which in return results in a low noise level and a high SNR. In practical terms, HDR enables high contrast and accuracy which finds itself many applications from security to industry. The proposed new smart solution is implemented within the pixel structure of a ROIC and includes two input amplifiers and a mechanism which selects the best performing input amplifier automatically according to the incoming illumination level. This solution is compatible with both high dynamic range SWIR and dual-band, multicolor detectors.

A 32×32 prototype is developed to present the new smart ROIC architecture. A 32×32 prototype is not hybridized with detector, instead process and temperature variation compensated current sources are used to mimic detector behaviour. It achieves current levels between 10 pA and 3 nA.

This paper is organized as following. After this introductory section, the smart ROIC architecture is given in Section 2. The practical design considerations and sub-block performances are discussed in Section 3. In Section 4, array design and measurement results are given. Finally, in Section 5, a comparison of the state of the art and the proposed smart ROIC architecture is given, concluding the manuscript.

2. Pixel architecture

Preamplifier which is located inside a unit cell is the first electrical interface between ROIC and detector, which is also responsible for the integration of current and charge to voltage conversion. The most critical part of the analog readout is preamplifier. Choice of preamplifier depends on many parameters such as frame rate, injection efficiency, and noise. Thus, SNR of the system is highly depending on preamplifier optimization.

Basic unit cell operation is shown in Fig. 1. Initially, reset switch is closed and the detector is biased between V_{det} and V_{reset} voltages. Integration operation immediately starts after the reset switch is opened. During integration, according to the incoming light level and the detector bias, DC current is integrated on the C_{int} capacitor. C_{int} consists of all the parasitic capacitances in that node, the input capacitance of the buffer, the integration capacitance and the interconnection capacitances.

Detector characteristics such as input impedance, detector bias and input current determine preamplifier topology. There are various types of preamplifiers, but most common ones are direct injection (DI), source follower per detector (SFD) and capacitive transimpedance amplifier (CTIA). Two critical parameters can be used to determine amplifier topology for a pixel. These are illumination level and readout frame rate. These parameters are used to determine well capacity and noise performance of the pixel.

In the smart pixel architecture, instead of using a single input amplifier; two input pre-amplifiers which are optimized for low and high photon flux levels are utilized. Fig. 2 represents the conventional and the smart pixel architecture. The smart pixel significantly diverges from the usual structure with extra amplifiers and an in-pixel smart control circuit. The control mechanism selects the best optimized input amplifier according to the incoming flux level. The smart control mechanism consists of latches and switches which occupy small pixel area.

CTIA and SFD input amplifiers, which respectively cover low and high illumination levels, are used in the SWIR smart pixel design. The choice of CTIA for the low illumination level is based on its injection efficiency of very low currents (low photon flux) and its low noise characteristic with the choice of small integration capacitance. The integration capacitance of CTIA can be very small unlike other topologies because the output of the unit cell is connected to the amplifier output which is a low impedance node. This yields reasonable noise performance [11].

The input referred noise of the CTIA is given by:

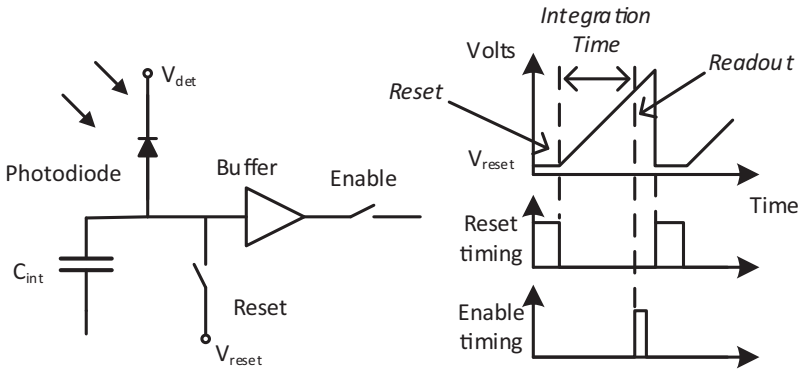

Fig. 1. Unit cell operation.

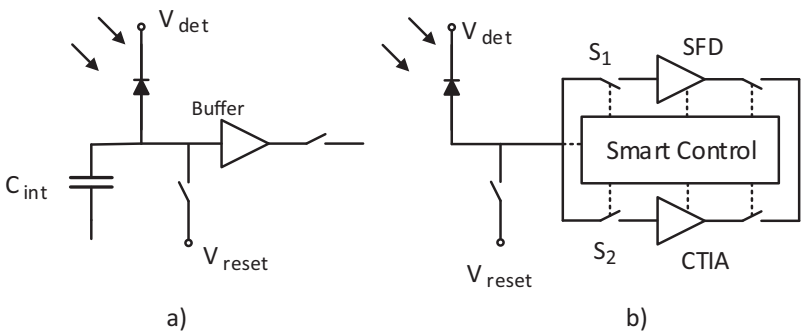

Fig. 2. (a) Standard pixel structure and (b) the smart pixel architecture.

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