Current Applied Physics 17 (2017) 327–332

Contents lists available at ScienceDirect

Current Applied Physics

journal homepage: www.elsevier.com/locate/cap

On the correlation of growth, structural and electrical properties of epitaxial Ge grown on Si by solid source molecular beam epitaxy

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ARTICLE INFO

Article history:
Received 12 August 2016
Received in revised form
7 December 2016
Accepted 22 December 2016
Available online 24 December 2016

Keywords:
Epitaxial Ge
MBE
CMOS
Photodetector

ABSTRACT

We report growth, structural, and electrical properties of epitaxial Ge layers on Si (001) wafers for next generation complementary metal oxide semiconductor devices. The epi-Ge layers were grown by solid source molecular beam epitaxy (MBE) at substrate temperatures (T_G) varying from 200 °C to 500 °C. A two-step growth process, where an initial layer of thickness ~30 nm is grown at a substrate temperature of 250 °C (except those grown below/at 250 °C), and the remaining layer is grown at a higher temperature, was found to be an efficient approach to improve the crystal quality of the Ge layers. The epi-Ge on Si exhibits bulk hole-mobility as high as 736 cm^2/V-s at room temperature. Ti/Ge/Ti metal-semiconductor-metal (MSM) back-to-back Schottky diodes, fabricated on these epitaxial Ge layers, show excellent electrical properties. Further, metal oxide semiconductor (MOS) capacitors fabricated with HfO_2 as the gate oxide exhibit low leakage current density of 4.7×10^{-2} A/cm^2 (at $V_g - V_{FB} = 1$ V) and mid-gap interface trap density of $5.0 \times 10^{12} cm^{-2} eV^{-1}$.

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1. Introduction

Germanium (Ge) is emerging fast as a material of choice for a variety of new technologies, such as high performance MOSFETs [1–3], near infrared (NIR) photodetectors [4,5], multi-junction solar cells [6], thermo-photovoltaics [7], and lasers [8]. Epitaxial growth of Ge thin films on silicon (Si) substrates is currently one of the frontiers in the opto- and microelectronics research, driven primarily by the scaling of logic devices beyond the 22-nm node and monolithic integration of photonic devices on the Si-CMOS platform [9–11]. Besides, relaxed Ge epilayers on Si serve as virtual substrates for integration of several III-V semiconductors and group-IV alloys [12,13]. The primary constraint of realizing high quality Ge epilayers on Si is the significant mismatch (~4.2%) between the respective lattice parameters [14], which results either in plastic relaxation of the growing epilayer by formation of misfit dislocations [15], or elastic relaxation by formation of islands (Stranski-Krastanow growth), leading to a rough surface [16,17]. Over the years, several sophisticated techniques have been developed to circumvent this issue, some of which often require high thermal budgets [18–21]. However, thermal treatments involving high temperatures may not be suitable process routes as it may lead to unequal distribution of tensile/compressive stress across the epi-Ge layer as reported very recently by Zhao et al. [22]. This limitation emphasizes the need to develop and optimize methods for Ge on Si epitaxy at low temperatures, which still continues to be a formidable challenge. By thermal evaporation of Ge in high vacuum environment, Colace et al. have demonstrated the possibility of performing Ge/Si (001) epitaxy at growth temperatures in the range of 300–400 °C [5]. Ge growth on Si(001) substrates at temperatures as low as 180 °C has been demonstrated very recently by Chang et al. using a technique called electron cyclotron resonance chemical vapor deposition (ECR-CVD) [23]. To the best of our knowledge, majority of the reports primarily focus on the growth of epi-Ge on Si substrate by various techniques under different process conditions.

The present work investigates the growth, structure and electrical properties of epitaxial Ge on Si (001) and explores the possibility of using the same for next generation complementary metal oxide semiconductor (CMOS) devices. Epitaxial Ge layers on Si (001) substrates were grown by solid state molecular beam epitaxy (MBE) at growth temperatures as low as T_G = 200 °C, and a

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http://dx.doi.org/10.1016/j.cap.2016.12.020
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systematic investigation of the crystalline quality, surface morphology, and electrical characteristics of the Ge epilayers was carried out. We show that Ge/Si (001) epitaxy at such low growth temperatures can result in very smooth surface morphology, however, at the cost of a higher dislocation density. A two-step growth process where a low temperature (~250 °C) growth of an initial layer (~30 nm) was followed by higher temperature growth (>250 °C) has been found to be far more effective in improving the crystal quality with significantly reduced dislocation density. Although, there are several reports [24–27] on epitaxial growth of Ge on Si by various methods including the low temperature growth followed by high temperature growth (LT-HT) approach, the earlier investigations were primarily limited to microstructural analysis with regard to the process conditions. Furthermore, the thicknesses of all the layers that were considered for these studies were mostly more than 1 μm. Though Nakamura et al. reported thin Ge layer (~130 nm) with smooth surface and low defects, the presence of ultra-thin SiO_2 layer to form Ge nanodots may have its own issue for further CMOS process. In the present work, we compile growth, structural, and electrical properties of the epi-Ge/Si layers of thicknesses around 600 nm, grown on Si by MBE. The thickness of Ge epi-layer was measured by Bruker Dektak XT profilometer. The layers have been investigated by several electrical methods, particularly to explore their potential towards next generation CMOS devices. Electrical characteristics of Metal (Ti)-Semiconductor (Ge)-Metal (Ti) (MSM) back-to-back Schottky diodes appraise the bulk electrical properties of these epi-Ge layers, while metal-oxide-semiconductor (MOS) capacitors with HfO_2 as the gate oxide evaluate their minority carriers properties and interface trap. We show that the Al/HfO_2/epi-Ge–Si (001) based MOS capacitors exhibit an excellent interface, with low interface trap density and leakage current. Based on the present study, we infer that these epi-Ge layers, grown at relatively low temperatures on Si(001) by MBE can be potential candidate for next generation Ge-based complementary metal oxide (CMOS) and optoelectronic devices integrated onto the existing Si-based technology.

2. Experiment

The Ge epitaxial films were grown on p-type (Resistivity: 1–10 Ω–cm) Si (001) substrates in a RIBER Compact 12 solid source MBE system, with a base pressure of 1×10^{-10} Torr. High purity Ge (99.9999%), contained in a standard Knudsen cell with a pyrolytic BN crucible, was used as the source. The Si (001) substrates were thoroughly cleaned by standard RCA techniques and hydrogen-passivated by treating with buffered HF solution, before loading in the loadlock of the MBE chamber. The substrates were then degassed inside the loadlock for 12 h at 180 °C and subsequently transferred to the growth chamber at ~150 °C. Prior to Ge growth, the substrates were heated up to 700 °C, which led to desorption of the hydrogen passivation layer and appearance of the desirable (2×1) surface reconstruction. Formation of the (2×1) surface reconstruction is very crucial for achieving a smooth surface in low temperature Ge/Si (001) epitaxy. For samples grown at 250 °C and above, the two-step growth process was followed. Approximately 30 nm of Ge was first grown at 250 °C and subsequently, the substrate temperature (T_G) was increased to higher values, while continuing growth. On the other hand, growth was performed at a single temperature for $T_G \leq 250$ °C. Reflection high energy electron diffraction (RHEED) images were recorded in real-time to monitor the surface, throughout the entire growth.

The crystalline quality of the Ge epilayers were investigated by high resolution X-ray diffraction (HRXRD), using Cu $K_{\alpha 1}$ emission of a Rigaku X-ray diffractometer. The strain state of the epilayers was further probed by Raman spectroscopy using a 514.5 nm laser. Information regarding the quality of the Ge/Si interface was obtained by high-resolution transmission electron microscopy (HRTEM), using a JEOL microscope. In order to further examine the electrical quality of the epi-Ge layers, room temperature Hall measurement was carried out. MSM back-to-back Schottky diodes were fabricated by patterning Inter-Digitated Electrodes (IDE) on the Ge epilayers, by single level optical lithography, metallization, and lift-off. Metal electrodes were deposited by e-beam evaporation of 30 nm of Titanium, and 200 nm of Gold. Further, MOS capacitors were fabricated by depositing 9 nm thick HfO_2 in a Cambridge Nanotech Fiji 200 atomic layer deposition (ALD) system, using tetrakis (dimethyloamido) Hafnium ($Hf(NMe_2)_4$) and H_2O as precursors. Before oxide deposition, the epi-Ge layer was cleaned with de-ionized water and iso-propyl alcohol and passivated by dipping in 2% HF solution. To fabricate the metal contacts, patterns were generated by standard optical lithography, reactive ion etching with CF_4, and e-beam evaporation of 150 nm Aluminum (Al). After metal deposition, the MOS structures were annealed at 400 °C in a 900 sccm forming gas (96% N_2 and 4% H_2) environment for 60 s. Electrical properties, such as capacitance-voltage (C-V) and leakage current (J-V) characteristics of the MOS capacitors were measured using an Agilent B1500A parameter analyzer.

3. Results and discussion

Real-time monitoring of the sample surface was done by recording RHEED images during and after completion of Ge growth. Fig. 1 shows the RHEED images recorded after growth of Ge layers at different growth temperatures. A streaky RHEED pattern indicates a smooth surface, characteristic of two-dimensional growth. Despite the large lattice mismatch (~4.2%) between Ge and Si, the surface of epi-Ge layer remains atomically sharp even during growth at higher substrate temperature (>500 °C). This

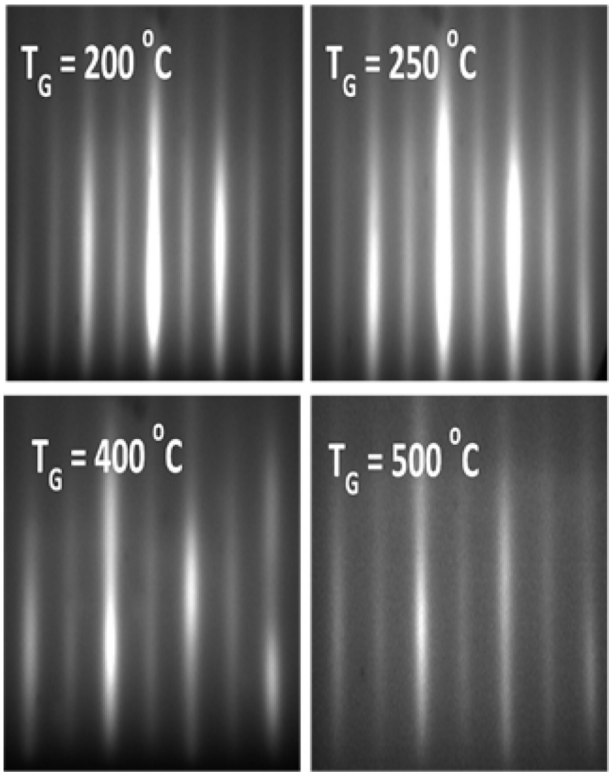

Fig. 1. RHEED images recorded at the end of Ge growth at different T_G, showing (2×1) reconstruction of the as-grown surface.

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