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Gate leakage current suppression and reliability improvement for ultra-low EOT Ge MOS devices by suitable HfAlO/HfON thickness and sintering temperature

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ABSTRACT

Ultra-low effective oxide thickness (EOT) Ge MOS devices with different HfAlO/HfON stacks and sintering temperatures are investigated in this work. The suppression of gate leakage current and improvement of reliability properties can be achieved by either stacked gate dielectrics or a low sintering temperature. Especially, the qualities of the interface and high-k gate dielectric in Ge devices are significantly improved through a low sintering temperature. A 0.5 nm HfAlO/2.5 nm HfON gate stack and a sintering temperature at 350 °C are the suitable conditions to achieve low EOT, gate leakage, and good reliability for Ge MOS devices.

1. Introduction

High-k gate dielectrics have been implemented for advanced metal-oxide-semiconductor (MOS) device applications. When the gate oxide becomes thinner, a reduction in carrier mobility is also encountered. Therefore, devices with a higher carrier mobility are desirable to improve the performance of MOS circuits [1]. Germanium (Ge) has been regarded as the most promising material for improving the MOS performance because of its higher electron and hole mobility, which are two and four times higher than silicon [2,3]. In order to implement high-mobility Ge MOS device, one of the most critical technology issues is to form a high-quality interfacial layer (IL) at high-k/Ge [4,5]. A uniform GeO_2 can serve as a good IL, and it has a sufficient wide band gap (almost 6 eV) and high barriers for electrons and holes [6].

The gate leakage current increment and reliability degradation are the two key issues while device scaling down [7]. For the high-k dielectric layer, HfO_2 has been the most promising material with a higher k-value and a larger band gap [8], but it is also easily crystallized during the thermal processes. It is well known that the more high-k layer crystallized, the more gate leakage current induced. In order to reduce the crystallization, a high-k with doping Al or a lower temperature thermal treatment may be good approaches for fabrication processes in Ge MOS devices. An ultra-thin HfAlO layer formed by doping Al into HfO_2 can help lower the crystallization of dielectric to fulfill the goal of gate leakage current reduction [7]. A thermal treatment at low temperature may also accomplish this goal. Therefore, Ge MOS devices with different HfAlO/HfON gate stacks and sintering temperatures are studied in this work.

2. Experiment

The fabrication processes of Ge MOS devices are started on an n-type Ge substrate (~5 Ω-cm) with (100) orientation. After dilute HF clean (1:100 for HF:DI water), GeO_2 IL is grown by using the H_2O plasma process within an atomic layer deposition system (ALD). Then, various thickness stacks of HfAlO/HfON gate dielectrics are in-situ deposited by the ALD. HfON is formed by precursor TEMAH $[(CH_3)(C_2H_5)N]_4Hf$ and H_2O plasma, and HfAlO is formed by precursors TEMAH, TMA $(CH_3)_3Al$, and H_2O plasma [9].

There are four samples in this work. The control sample is the one without any Al doping. The other three samples with a total thickness of 3 nm are formed by 0.5 nm HfAlO/2.5 nm HfON, 1 nm HfAlO/2 nm HfON, and 1.5 nm HfAlO/1.5 nm HfON, respectively. The following metal gates with 30 nm TaN are deposited by a sputtering. Then, metallization with 300 nm Al is deposited by a PVD. Lithography and gate etching are followed to define the active region. The sintering process is performed on these devices at 400 °C for 30 min.

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Table 1
Split conditions of devices with different HfON/HfAlO stacks and different sintering temperatures.

Device ID	Control	S1	S2	S3	300	350
Metal gate	TaN 30 nm				TaN 30 nm	
Gate dielectric	HfON 3 nm	$HfAlO_2$ 0.5 nm HfON 2.5 nm	$HfAlO_2$ 1 nm HfON 2 nm	$HfAlO_2$ 1.5 nm HfON 1.5 nm	HfON 3 nm	
Interfacial layer	GeO_2 (by H_2O plasma)				GeO_2 (by H_2O plasma)	
Substrate	N-type Ge substrate				N-type Ge substrate	
Temp. of sintering	400 °C				300 °C	350 °C

The sinter processes at different temperatures are performed on samples with the same IL and 3 nm thick HfON in-situ deposited by an ALD system. Then, 30 nm thick TaN metal gates are deposited by a sputtering. After metallization, lithography, and gate etching processes, sintering is performed at 400 °C, 350 °C and 300 °C, respectively. The detailed split conditions are shown in Table 1. Samples with various gate dielectric stacks are denoted as S1, S2, and S3; while 300 and 350 represent different sintering temperatures. Fig. 1 shows the process flow and schematic cross-section of Ge MOS devices in this work. All the stress conditions for reliability tests are performed at 3.3 MV/cm.

3. Results and discussion

Fig. 2 shows capacitance versus applied voltage (C–V) curves of Ge MOS devices with different HfAlO/HfON stacks measured by HP4284 instrument from −1 V to 2.5 V at 100 kHz. The equivalent oxide thickness (EOT) is extracted by the CV simulation. By this method, the EOT and flat band voltage (V_{FB}) can be fitted. Quantum and gate depletion effects are also considered in this simulation.

The accumulation capacitance of control sample is about 4.57 μF/cm^2, and that of sample with 1.5 nm HfAlO (S3) is 3.25 μF/cm^2. Results indicate that doping Al into HfO_2 decreases a little capacitance due to the lower k-value of Al_2O_3. Furthermore, the more Al doped into HfO_2, the more V_{FB} shifted to the right. It may be due to some Al-induced negative oxide traps.

Fig. 3 shows leakage current densities (J_g) of Ge MOS devices with different HfAlO/HfON stacks measured by HP4145 instrument from −0.75 V to 1.5 V. It is found that the J_g decreases with increasing the thickness of HfAlO layer in HfAlO/HfON stacks. The leakage current density at $V_g = V_{FB} + 1$ V of control sample is 2.58 A/cm^2, and that of S3 sample is 5×10^{-1} A/cm^2. It indicates that doping Al into high-k can suppress the crystallization and reduce the leakage current, but it also increases EOT as shown in Fig. 2. In addition, Al doped HfO_2 may also form a larger band gap offset to prevent thermal emission effects [10].

The cumulative probabilities of J_g for Ge MOS devices with different gate stacks are shown in Fig. 4. It is clear that the uniformity is improved for samples with HfAlO layer in gate dielectric stacks. The J_g values of samples with HfAlO layer in gate dielectric stacks are ~1 A/cm^2 and uniform; while that of control one is 1–10 A/cm^2.

Fig. 5 shows scaling trend of J_g versus EOT for Ge MOS devices with benchmarks. The gate leakage current is reduced to 5×10^{-1} A/cm^2 and the EOT is only increased for approximately 0.15 nm. The trend lines are slightly below those in the recent papers [7,11].

Fig. 6 shows stress-induced V_{FB} shifts of Ge MOS devices with different HfAlO/HfON stacks. It is found that stress-induced V_{FB} shifts for samples with HfAlO in gate dielectric stacks are increased. The V_{FB} shift of sample with 0.5 nm HfAlO (S1) is about 0.05 V, which is almost equal to that of control sample. Thus, sample with little or suitable HfAlO in gate dielectric can have few oxide traps.

Fig. 7 shows stress-induced gate leakage current of devices with different HfAlO/HfON stacks. It is observed that all samples with HfAlO in gate dielectric can suppress the gate leakage current about 8% compared with the control one. The SILC values of samples with 1 nm and 1.5 nm HfAlO (i.e. S2 and S3 samples) are larger than that with 0.5 nm HfAlO (S1 sample). Hence, sample with 0.5 nm thick HfAlO in gate dielectric stack shows the lowest SILC. Since the sample with 0.5 nm thick HfAlO in gate stack has quite small stress-induced V_{FB} shift as mentioned in Fig. 6, it demonstrates the best reliability characteristics in this work [12].

Fig. 8 shows C–V curves measured by HP4284 instrument from −1 V to 1.5 V at 100 kHz of HfON gated Ge MOS devices with sintering temperatures at 400 °C, 350 °C and 300 °C, respectively. It is seen that the capacitances are little changed for different sintering temperatures. With sintering temperature from 400 °C to 300 °C, the EOT value increases a little from 0.39 to 0.41 nm. The V_{FB} increases a bit with decreasing sintering temperature from 400 to 300 °C. Therefore, a lower sintering temperature may result in less crystallization in dielectric layer so that the EOT is increased.

Fig. 9 shows J_g of HfON gated Ge MOS devices with different sintering temperatures. The leakage currents are almost the same in the accumulation region. The sample with a lower sintering temperature shows a slightly lower leakage current density. This again can be

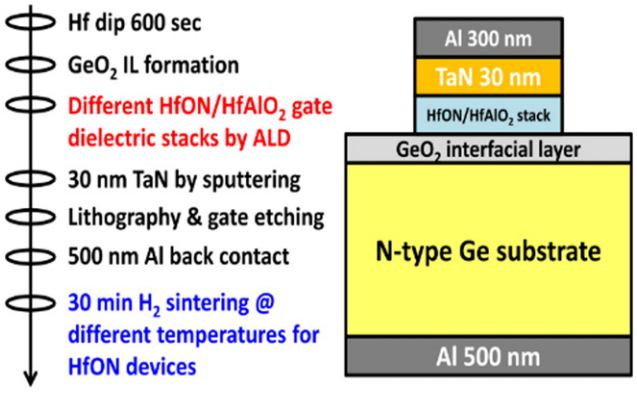

Fig. 1. Fabrication processes and schematic cross-section of devices.

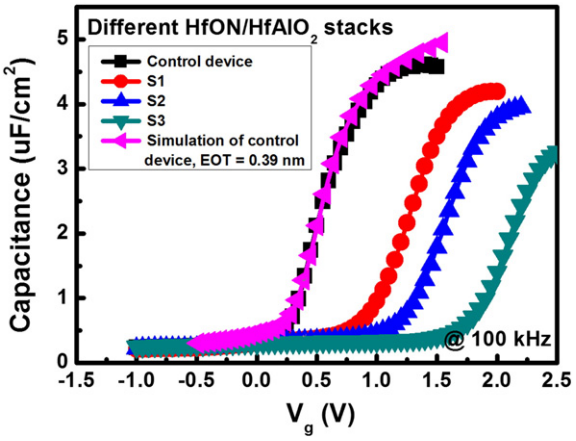

Fig. 2. CV curves of Ge MOS devices with different HfON/HfAlO stacks.