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Heat stress exposing performance of deep-nano HK/MG nMOSFETs using DPN or PDA treatment

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ABSTRACT

Decoupled plasma nitridation (DPN) or post-deposition annealing (PDA) process after high-*k* (HK) deposition to repair the bulk traps or the oxygen vacancy in gate dielectric is an impressive choice to raise up the device performance. Before heat stress, the electrical performance in drive current, channel mobility and subthreshold swing with both treatments was approximate, except the higher annealing atmosphere causing the thicker interfacial layer and reducing the overall related dielectric constant. After temperature stress, the electrical performance for all of the tested devices was slightly deteriorated. The degradation degree for electrical performance with PDA treatment group was the worst case due to NH_3 atmosphere forming Si–H bond on the channel surface, which was broken after stress and produced more interface state reflected with the increase of subthreshold swing.

1. Introduction

On behalf of Si-based semiconductor industry, the shrinkage of metal-oxide-semiconductor field-effect transistor (MOSFET) in channel length or gate dielectric thickness is an effective option to promote the drive current, but possibly causing more tunneling gate leakage and device reliability problems. To solve these vexatious issues of conventional SiO_2-based gate dielectric approaching their physical limits, at the 45-nm node technology generation, high-*k*/metal gate (HK/MG) technologies [1–3] have been introduced to reduce the exponentially increasing gate leakage and raise the transistor performance. Hafnium-based dielectric is one of most promising gate dielectric materials replacing silicon dioxide or oxynitride due to high relative dielectric constant (*k*-value), acceptably thermal stability, low mobility degradation and superior gate leakage. Utilizing metal gate engineering eliminates gate poly-silicon depletion and relatively reduces the electrical equivalent oxide thickness (EOT). Additionally, only using high-*k* material with gate poly-silicon easily induces Fermi-level pinning [4], lower carrier mobility and RC delay problems. Therefore, instead of HK/MG technology is able to soften the previous phenomena.

Due to the previous considerations, the high-*k*/metal gate stacking supplanting the oxynitride/poly-gate can validly suppress the variation of threshold voltage. Some of the latent issues associated with the high-*k* dielectrics, however, demonstrate such as larger amount of oxygen vacancy [5,6] in high-*k* dielectric possibly increasing gate leakage [7,8] and deteriorating the device performance after long-term operation and inferior quality of surface bonding between high-*k* dielectric and silicon channel [9,10]. Using a stacked dielectric [11] replacing pure high-*k* deposition as well as the formation of interfacial layer (IL) between high-*k* and surface channel is a good choice to reduce the gate leakage and the carrier scattering coming from surface roughness or interface states and possibly increase the crystallization temperature of gate dielectric. Furthermore, if the nitridation treatment [12] after high-*k* deposition is adopted, the drive current due to the repair of oxygen vacancy in high-*k* dielectric is effectively increased. Finally, in

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reliability perspective, the trap charges [13] in gate dielectric or interfacial layer need to be carefully treated in the future.

2. Formation of MOSFET devices

The integration process in this work accompanied a standard frontend-of-line (FEOL) CMOS process flow up to Hf-based ($HfZrO_x$) HK dielectric layer deposition. To retard the amount of oxygen vacancy and slightly increase the dielectric constant contributing the drive current, employing an economic post deposition annealing (PDA) [14] or high-efficiency decoupled plasma nitridation (DPN) process [15] to obliquely control the amount of oxygen vacancy in HK layer is a useful alternative. In addition, the HfOx/ZrOy/HfOx (HZH) [16] gate dielectric with atomic layer deposition (ALD) technique [17,18] was layer-by-layer to be formed after the interfacial layer (IL) of silicon oxide ≈9–12 Å was thermally grown. The other key process engineering contains Si-based substrate, channel implantation, source/drain (S/D) engineering, interfacial layer, barrier metal, and low-resistivity Al metal gate. The schematic cross-section profile of a nano planar MOSFET device is depicted in Fig. 1. Considering the promotion of the drive current in MOSFETs, there are two common strain technologies [2] in nano-node process: stress memorization technique (SMT) and contact-etch-stop-layer (CESL) process beneficial to n-channel MOSFET (nMOSFET or NFET) device and embedded SiGe S/D plus replacement metal gate (RMG) technique helpful to p-channel MOSFETs. After the deposition and shape formation of barrier metal adjusting the work function (WF) and metal gate were done, the contact and backend-of-line (BEOL) processes were followed with the matured traditional CMOS process flow. The whole 28-nm HK/MG process flow with gate-last (GL) process with the equivalent oxide thickness (EOT) ≈26 Å is shown in Fig. 2 [19].

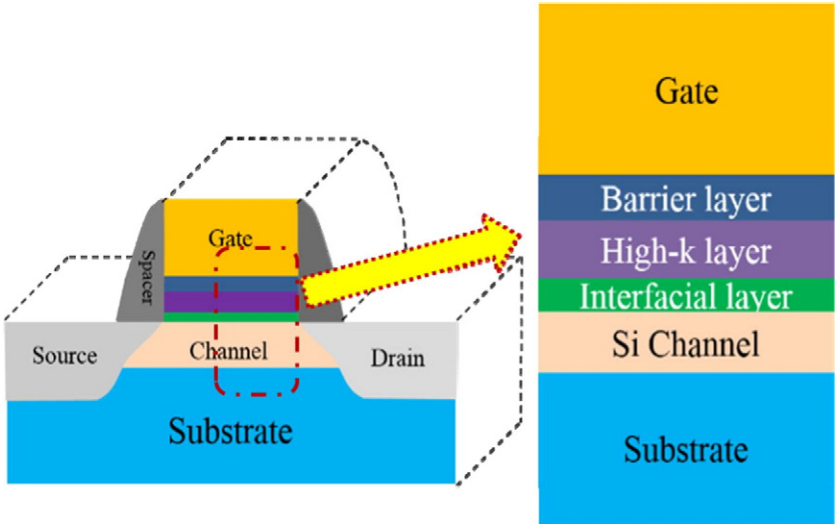

Fig. 1. Schematic cross-section profile of an nMOSFET.

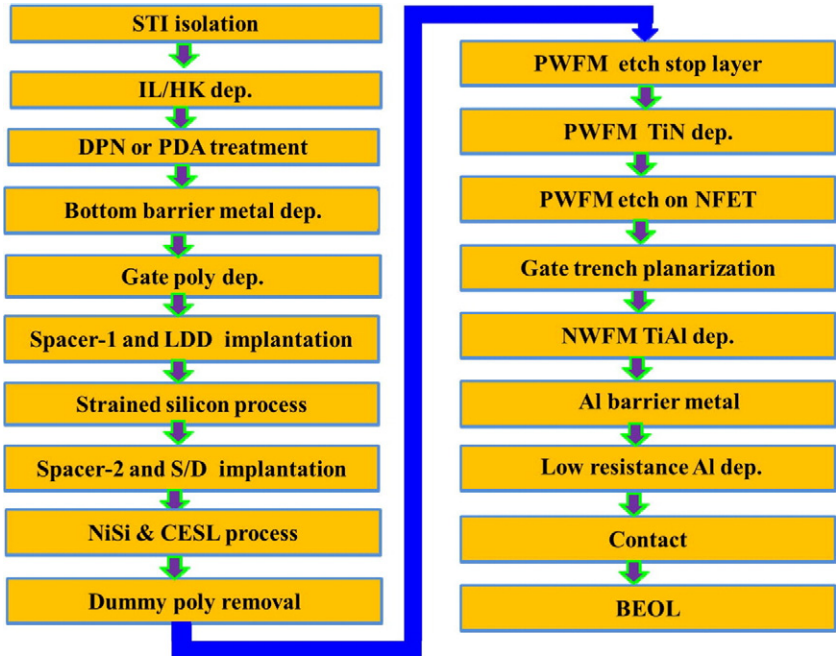

Fig. 2. Simple process flow of 28 nm gate-last MOSFET devices.