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Mechanical grooving effect on the gettering efficiency of crystalline silicon based solar cells

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ABSTRACT

This paper examines a gettering process of Czochralski silicon (CZ) via mechanical texture, followed by two step heat treatment in the presence of porous silicon layer (PSL) under oxygen flow gas. It is shown that a process with PS has a positive trend of improvement in the electronic quality, and found to be more efficient when used in combination with mechanical grooving. We obtained a significant increase of the effective minority carrier lifetime and majority charge carriers mobility. Thus, there is an apparent decrease in the resistivity. These parameters were estimated through a The Quasi-Steady-State Photo-Conductance technique (QSSPC), the van Der Pauw method and Hall Effect. Particularly, we have made obvious that the large enhancement of the electronic quality of the wafers can be related to the presence of grooves, the influence during which the gettering process is of importance to overcome the unexpected saturation phenomena. The current voltage I-V characteristics of all samples had been measured under illumination. They were shown to enhance the photovoltaic properties of solar cells.

1. Introduction

Crystalline silicon [c-Si] has become the main material in the photovoltaic market. Single crystalline substrates are typically differentiated by the process by which they are made. Czochralski (Cz) wafers are the most commonly used type of silicon wafer, and are used by both the solar and integrated circuit industry. The Czochralski-technique is a method by which means a monocrystal is pulled with the same crystallographic orientation of a small monocrystalline seed crystal out of melted silicon. The electrical properties of c-Si wafers degrade due to the presence of impurity atoms and defects. Metallic impurities have a negative impact on c-Si solar cells, due to their detrimental effect on carrier lifetimes and mobility. Such metals may be present in numerous forms, including substitutional or interstitial ions. It has been shown by Kveder et al. [1] that the interaction between impurities in bulk c-Si may provide very efficient recombination centers. The negative impact of these impurities can often be reduced by phosphorus or aluminum gettering [2,3]. It is needful to remove these impurities by external gettering techniques because solar cells have sensitivity to whole bulk c-Si [2]. Nevertheless, more recently porous silicon layers (PSLs) had also been used as an efficient sacrificial layer for gettering metallic impurities. The PSLs were demonstrated as surprising properties which could help in the development of electricity applications [4].

The known gettering techniques are usually very effective at removing interstitial impurities, and improvements in lifetime minority carrier [5]. However, more recent experiments performed on c-Si wafers indicated that it was possible to significantly reduce the defect and impurities density by a high temperature gettering or efficient surface treatments [6,7]. The combination of such methods includes gettering in the presence of aluminum into PSLs or phosphorus-rich PSLs [8,9]. In all cases, these combination processes demonstrate the possibility to mitigate the impact of such defect on solar cells devices [8–12]. The challenge to reduce the deleterious effect of the defects on devices without introducing costly processing steps can be achieved in this work.

The aim of this work is to study the combined effect of mechanically textured surface and treated PSLs at high temperature under O_2 flow gas. It was shown that there is a quasi-saturation level when the treatment period exceeds 40 min [13,14]. It may be

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adequate to make the process for short annealing durations, and repeat it two times.

We investigated the role of grooves in the presence of PSLs is enhanced at the front surface on the gettering experiment efficiency. This novel approach could be a powerful technique for efficiency gettering.

2. Experimental procedure

The used substrates are Czochralski (Cz) solar grade (SG) (1 0 0) oriented, p-type boron doped silicon, with a resistivity ranging from 1 to 2 Ω cm. The samples were selected from adjacent slocations from the ingot to ensure that crystal defects were closely matched. Silicon wafers with initial contamination levels, ranging from 10^{13} cm^3 to 10^{16} cm^3 (medium) [15]. All wafers were diced into quarters having an area of 4 cm^2 and were divided into two sets. A specific process was applied in the first set by mechanical grooving. This texturization consisted of parallel grooves with spacing 100 μm, and many trials for different values of mechanical parameters were carried out. On the basis of these trials optimum parameters of mechanical texturization were adjusted and assumed to take the following values: speed of the mechanical scan v = 0.5 mm/s, and a groove width of 10 μm. A chemical surface treatment after mechanical texturisation was performed to remove mechanical damaged layer throughout porous silicon formation. Immediately after PS formation, the samples were rinsed with distilled water and dried under N_2 flux, to prevent the PS film from flaking and deterioration. The second set still ungrooved. Then, thin PSLs were formed on both sides for all samples by stain-etching in HF/HNO_3/HO solution with 1:3:5 vol compositions allowing the cleaning of the mechanical damage. Thereafter, the samples of PSLs with and without grooves were thermally annealed in an infrared furnace under oxygen (O_2) flow gas at temperatures of 600 °C, 700 °C, 800 °C and 900 °C, the annealing duration is 40 min. After each annealing steps, we studied the effect of the treatment after removing the sacrificial PSLs. We note that in order to eliminate the forming silicon oxide layer and to remove the PSLs, we immersed these samples successively in an HF (5%) and NaOH (1 M) solutions. Further, substrates of both grooved and ungrooved sets were subjected to an iterative gettering: two step gettering process. But, before proceeding to the second annealing step, the PSLs were renewed. They were removed after finishing these second treatments.

Firstly; surface morphology were determined by a scanning electron microscope (SEM). Then, the surfaces of the wafers must be sufficiently passivated to allow bulk recombination lifetime measurements. The di-iodine–ethanol (I–E) mixtures solution (0.1 M) used for few minutes providing some surface passivation before lifetime measurement [16]. Furthermore, the minority carrier lifetime was measured using a Sinton WTC-120 set-up (reference) with the intention to evaluate the heat treatment effect as well.

Secondly, the resistivity and Hall mobility of holes were measured by the Hall Effect method [13] at troom temperature with typical values of current density and magnetic field respectively equal to 0.5 mA and 0.15 T. However, the four points of contacts were achieved by thermal evaporation of aluminum at 10^{-6} mbar.

Finally, the c-Si solar cells were achieved by performing the phosphorus diffusion technique at 925 °C for 30 min. The back contact (Ag/Al) and the front contact (Ag) were produced by screen printed and fired at 850 and 620 °C respectively. The electrical characterization (I–V) was measured by a source meter Keithley 2400 under illumination. The topography of the surface after each process was studied using Scanning electron microscopy (SEM). The data was analyzed by software origin.

3. Results and discussion

3.1. Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) plan view of treated samples surface is presented in Fig. 1.

Fig. 1(a) depicts the untreated silicon surface. The porous silicon structure fabricated by stain etching was shown in Fig. 1 (b) as having a spongy structure rich in pores (empty) and disorders compared to the bulk silicon. Fig. 1(c) depicts the textured surface by mechanical grooving. As illustrated in Fig. 1(c), the mechanical grooves increase the surface area thereby making porous silicon chemically more reactive. This figure confirms the appearance of mechanical stresses on silicon surface.

After observing Fig. 1(d), one can find that the PSL treated at high temperatures for 40 min leads to change the pore size on the silicon surface. Further, the SEM shows that the PSLs recrystallize through the coalescence of pores, and the crystal defects are diminished during the oxidation cycles at high treatment [17].

Fig. 1(e) shows that the porous surface is transformed further to an almost pore free and smooth surface without removing the grooves. However, the mechanical grooving ensures an increased number of damaged sites produced in the wafer during the oxidation cycles at high treatment.

3.2. Minority carrier lifetime

Fig. 2 illustrates the variation of the effective minority carrier lifetime τ_{eff} at an injection level of 10^{15} cm^{-3} for each treatment after samples being immersed in 0.1 M concentrated I–E solution. Nevertheless, the surface passivation is one of the most important parameters for the solar cell characterization.

From Fig. 2, it is obvious that the lifetime increases and presents an apparent dependence with the treatment conditions.

We notice an apparent enhancement of τ_{eff}. The lifetime was found to increase in grooved substrates, indicating that grooves have a beneficial effect on the gettering process and the efficiency of the gettering process is found to be more pronounced after the two step gettering process. It is figured out that the τ_{eff} is enhanced by increasing the effectiveness of the gettering sites. It is worthy to note that the gettering at high temperature annealing has enhanced the impurity diffusion into the sacrificial porous silicon layer as well as toward the grooved region. Mechanical damage gettering relies on the dislocations generated in silicon wafer depth and approached to the sinks the vicinity of the impurities located in the bulk silicon. However, it is important to note that the structure of PS were degraded with heat treatments; hence, this degradation may limit the getter efficiency.

3.3. Hall effect measurements

Figs. 3a and 3b are demonstrative of the dependence of the resistivity and mobility variation with temperatures as well as with the number of annealing steps. The resistivity and mobility are measured using the van der Pauw method and Hall Effect investigations. The measured values seem to be directly affected by the final impurities levels in the bulk leading to a strong correlation between resistivity and impurities density [18]. The resistivity decreases whenever the annealing temperature increases and this behavior is found to be more sensitive after the use of the two annealing step, especially in the groove samples.

The majority-carrier mobility evolution can be depicted in Fig. 3b. We can deduce that the majority-carrier mobility increased with increasing temperature. We note that the enhancement of the majority-carrier mobility comes from the gettering using