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Planar avalanche photodiodes with edge breakdown suppression using a novel selective area growth based process

O.J. Pitts [a,*], M. Hisko [a], W. Benyon [a], G. Bonneville [b], C. Storey [b], A.J. SpringThorpe [a]

[a] National Research Council Canada - Information and Communications Technologies, Canadian Photonics Fabrication Centre, Ottawa, Ontario K1A 0R6, Canada
[b] National Research Council Canada - Information and Communications Technologies, Electronics, Ottawa, Ontario K1A 0R6, Canada

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ABSTRACT

We propose and demonstrate a novel process to fabricate planar avalanche photodiodes using selective area growth (SAG) followed by a single Zn diffusion through the SAG material using the same dielectric mask. The tapered surface profile of the SAG epitaxy due to the enhancement of the growth rate in the vicinity of the mask edge modifies the diffusion profile, resulting in a gradual reduction of the diffusion depth towards the outer edge of the active area. The associated reduction of the electric field counteracts the edge curvature effect sufficiently to suppress edge breakdown. For undoped InP SAG epitaxy, small areas of higher electric field occur where the mask edge is along the [1 0 0] or [0 1 0] directions, associated with the formation of enhanced ridges in the SAG material in these locations. Similar ridges are observed for Si-doped InP and InP/InGaAs/InP SAG structures, but the enhancement of the electric field in these locations is significantly lower.

1. Introduction

Planar InGaAs-InP avalanche photodiodes (APDs) have been deployed in both 2.5 Gb/s and more recently, 10 Gb/s optical receivers [1–3]. Due to their buried p-n junction, planar-type APDs exhibit low dark current and high reliability compared to mesa-type APDs [3]. However, special attention to the design is needed to avoid early breakdown at the lateral junction periphery due to the enhancement of the electric field by the curvature of the p-n junction. Edge breakdown suppression has been reported using a combination of a stepped diffusion profile and floating guard rings (FGRs) fabricated either using a double diffusion process [2,4,5], or by a single diffusion with wet chemical recess etching of the central junction area [3,6,7]. However, edge breakdown suppression using either of these approaches is critically dependent on the p-n junction depth offset between the central and peripheral area. This offset is challenging to control reproducibly, requiring precise calibration of two diffusions performed at separate times in the double diffusion approach, or a precisely defined etch depth using the recess etch technique. Deviations of the depth offset from the design target may introduce enhanced electric fields either at the edge of the central region, or in the guard ring area [8]. In this work, we investigate an alternative approach using a selective area growth (SAG) process to modify the surface profile prior to diffusion. A single diffusion is then employed to form a p-n junction with a gradual transition from the central active region to the outer periphery, reducing the electric field sufficiently to avoid enhanced gain at the edge. We demonstrate suppression of edge gain for APDs fabricated using this technique both with and without guard rings.

2. Device structure and fabrication

The epitaxial structure of the APDs is based on the separate absorbtion, grading, charge, and multiplication (SAGCM) structure shown schematically in Fig. 1. The epiwafers were grown by metalorganic chemical vapor deposition (MOCVD) at 650 °C on S-doped InP substrates and consist of a Si-doped buffer layer, InGaAs absorption layer, InGaAsP step-graded region between the InGaAs and the Si-doped InP charge sheet layer, followed by a non-intentionally doped InP cap layer. The intermediate five layers of the step graded region were each 30 nm thick lattice matched InGaAsP with nominal photoluminescence wavelengths of 1.52, 1.39, 1.26, 1.13 and 1.10 μm. The non-intentional background doping is of the order of n ~ 1E14 cm^{-3}. All MOCVD process steps were performed in a Thomas Swan close coupled showerhead (CCS) MOCVD reactor. TMIn, TMGa, AsH_3 and PH_3 were used as the precursors for epitaxy, with Si_2H_6 used for n-type doping. The growths and diffusion were carried out with a reactor pressure

* Corresponding author.
E-mail address: oliver.pitts@nrc-cnrc.gc.ca (O.J. Pitts).

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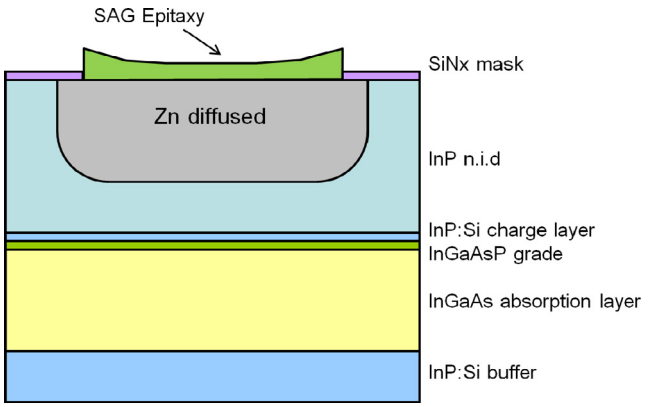

Fig. 1. Schematic structure of the APD device. After depositing the diffusion mask, the SAG epitaxy is performed first, then Zn is diffused through the SAG layer.

of 100 Torr and a total hydrogen gas carrier flow of ~21 L/min. A single dielectric mask was used for both the SAG process and the subsequent diffusion. The mask was fabricated from PECVD-deposited silicon nitride patterned by standard photolithography. The mask included devices both with and without FGRs in order to compare results for both types. The SAG epitaxy was performed by MOCVD at a growth temperature of 580 °C. Three different SAG epitaxial structures were compared: Structure A - 200 nm undoped InP; Structure B – 200 nm Si-doped InP; and Structure C – 50 nm InP/30 nm InGaAs/50 nm InP (all Si doped), where the thicknesses are given as the unenhanced or planar growth values. The diffusion process was also performed in the MOCVD reactor, in a separate process step, at 530 °C using DMZn as the Zn source with an over-pressure of PH_3 to prevent desorption of phosphorus from the InP surface. The diffusion process conditions were chosen so to produce devices with low dark current [9] and to prevent solid Zn_3P_2 deposits on the surface [10]. After diffusion, a rapid thermal anneal (RTA) treatment in a N_2 ambient was used in order to ensure electrical activation of the Zn dopant. Pd/Zn/Pd/Au ohmic p-metal contacts and Ti/Pt/Au interconnects/bond pads were then deposited. The characterization reported in this work was performed at wafer level after completing top side processing – n-side contact for electrical measurements was made through the n-type substrate without metallization.

3. Results and discussion

For each SAG epitaxial structure type, a wafer was cleaved along the $(1\bar{1}0)$ plane after completing the diffusion and RTA steps. The cleaved wafers were imaged by scanning electron microscopy (SEM) without any delineation etching, the electron yield difference from p and n regions providing sufficient contrast to image the shape of the junction and determine the diffusion depth, as shown in Fig. 2. The lateral diffusion of reactant species across the mask leads to a higher growth rate in the vicinity of the mask edges during SAG growth [11], resulting in the observed tapered thickness profiles. Due to the raising of the surface profile in the vicinity of the mask edges, the diffusion front is gradually curved upward over a distance of approximately 10 μm as it approaches the lateral edge. The increase in multiplication width near the outer edge, compared to the centre of the device, is approximately 0.15 μm for structure A, and 0.3 μm for structures B and C. This more pronounced effect of the SAG-enhanced edge region on the diffusion front is consistent with the lower diffusion rate of Zn in Si-doped InP and InGaAs, compared to unintentionally doped InP. The effect of Si doping on the Zn diffusion rate has been experimentally observed and explained in terms of a model in which

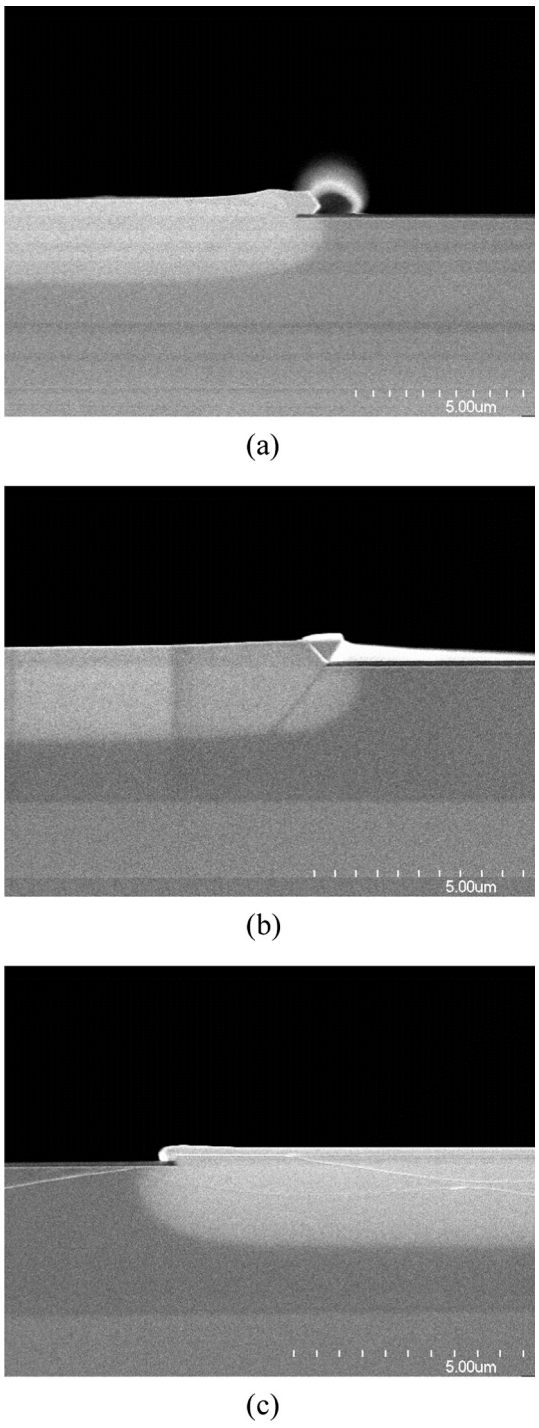

Fig. 2. Scanning electron microscope cross-section images of the diffusion front near the mask edge devices without guard rings, for wafers processed with (a) SAG structure A, (b) SAG structure B, (c) SAG structure C.

mobile Zn species diffusing into the Si-doped layers are immobilized by the formation of Zn-donor pairs [12]. As the Zn doping level near the surface after diffusion, 2-3E18 cm^{-3}, is significantly greater than the Si doping level, the SAG material is p-type in the completed devices and dopant compensation is not expected to have a significant effect. The multiplication width in the centre of the devices is in the range of 1.1–1.3 μm.

Fully processed wafers were characterized using dark and photocurrent I-V measurements. The dark and white light photocurrent I-V curves for a device on a wafer with SAG structure C are