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MOVPE growth of GaP on Si with As initial coverage

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ABSTRACT

The growth of a GaP 50 nm layer on Si by metalorganic vapor phase epitaxy is studied using AsH_3 and PH_3 pre-exposure at low (550 °C) and high (800 °C) growth temperatures. The samples are characterized by transmission electron microscopy. The results obtained reveal that the use of As as a first coverage layer on top of misorientated Si-substrates favors the formation of a defect-free GaP epitaxial layer, for a wide range of AsH_3 pre-exposure times using high growth temperature (800 °C), even though relatively low Si substrate annealing temperatures are used (850 °C) and no homoepitaxial Si layer was first grown. The procedure presented in this work reduces the thermal budget and complexity compared to most previous GaP/Si routines.

1. Introduction

The integration of III-V semiconductors on silicon has been suggested as a promising technology to reduce the cost of optoelectronics, solar cells and high speed electronics, due to the optical and electronic functionality of III-V semiconductors combined with the mature and low cost silicon-based microelectronic technology [1,2]. For all the applications mentioned above, the suitable III-V materials exhibit a large lattice mismatch to Si which hinders their integration. For example, for multijunction solar cells the maximum theoretical efficiency for a III-V semiconductor on Si Dual-Junction Solar Cell (DJSC) is 40% for a $GaAs_{0.8}P_{0.2}$/Si solar cell [3] which presents a 3.24% lattice mismatch between both materials. A common approach is the formation of a virtual III-V substrate, by growing a GaP nucleation layer on the Si-substrate, acting as a template for the growth of the complete III-V semiconductor structure since this heteroepitaxial growth (GaP/Si) has the minimum lattice mismatch for a III-V on Si, i.e 0.36%. However, the system (GaP/Si) presents certain challenges that degrade the quality of the layers: i) the epitaxial strain or three dimensional growth, that leads to the formation of defects at the GaP/Si heterointerface or/and in the epitaxial layer [4–6]; ii) the growth of a polar III-V semiconductor (i.e. GaP) on a nonpolar substrate (i.e. Si) induces the formation of antiphase domains (APD) [5–9], which, if they are not annihilated or avoided will be detrimental for devices; and iii) the unwanted cross doping through the interface [9]. Recent and very promising studies opened the possibility of modifying the surface of a Si-substrate by As-coverage (close to 1 ML) and thermal treatments previous to the GaP deposit [10].

The development of well-controlled growth procedures to achieve defect free GaP layers on Si is thus critical for the performance of the final devices and for industrial development.

The main requirements to achieve a successful growth of GaP on Si according to the literature are: i) the achievement of a clean Si surface free of any contaminants, especially C and O, since they can behave as nucleation centers for defects at the GaP/Si interface and ii) the formation of a single domain Si surface before III-V growth to avoid the formation of antiphase domains (APDs).

To achieve a clean Si surface most authors suggested a thermal treatment at high temperature (above 850 °C) under hydrogen not only to obtain an oxide and carbon-free surface but also to achieve double-step reconstruction on the Si wafer [5,6,9–14]. Some other authors also use homoepitaxial Si growth to bury any residual contaminant [4,7,8,15,16]. This last approach requires As-clean MOVPE reactors, and consequently growth interruptions and/or multi-reactor processes.

For the formation of a double-stepped Si surface to avoid APDs, the most common strategy is the use of misoriented Si wafers to enhance the formation of double steps at high temperature [5]; once this is achieved, the Si surface is pre-exposed to either group III or V elements in order to favor the formation of a given reconstruction of a Ga, As or P monolayer (ML). Regarding this pre-exposure or pre-nucleation step there is a wide range of approximations reported; how different pre-exposures affect subsequent growths has also been studied [17]. In MOVPE growth, most routines are based on group-V pre-exposure since the adsorption of group V elements with high vapor pressure on the surface is a self-limited phenomenon, contrary to exposure to group III atoms that tend to form clusters. The use of a P ML, either at high temperature [12–14] or low temperature [7,8,15] has been the most commonly reported strategy. In those cases in which low temperature

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Table 1
Description of the pre-exposure routine for each sample.

Sample	Pre-exposure			
	Group V	Time (s)	Temp (°C)	Flow (moles/s)
As–30 s-800C	AsH_3	30	800	$7.43{\cdot}10^{-6}$
As–360 s-800C	AsH_3	360	800	$7.43{\cdot}10^{-6}$
P–30 s-800C	PH_3	30	800	$3.71{\cdot}10^{-4}$
P–30 s-550C	PH_3	30	550	$3.35{\cdot}10^{-4}$
As–30 s-550C	AsH_3	30	550	$7.43{\cdot}10^{-6}$

GaP growth is required, tertiarybutylphosphine (TBP) is needed for an efficient pyrolysis of the P precursor. In comparison, only few works are based on As ML [6,10,11,18]. Just recently, the use of AsH_3 at high temperatures has been reported as giving promising results with Si substrate annealing below 850 °C [18]. In that work, the Si surface was exposed to AsH_3 at temperatures between 690 and 740 °C.

All these factors mentioned before increase the growth complexity, due to the time consumption, the thermal budget and the specific equipment requirements, making difficult the integration of GaP on Si technology with the standards required for the industry. Additionally, the number of parameters involved in the achievement of a defect free GaP layer is quite large (growth mode -continuous or pulsed-, growth temperature, pre-nucleation, etc) making the reported results non-easily transferrable to industry or even to other research reactors.

Accordingly, the main goal of this work is to set the basis for developing a GaP-on-Si growth procedure with: i) a lower thermal budget by reducing the Si annealing temperature; ii) one step growth (no reactor changes or growth interruption); and iii) wide range of growth parameters.

In order to determine the limits of the growth parameters that allow a defect-free GaP/Si growth and to have a deeper understanding of the nucleation process, the AsH_3 pre-exposure time and growth temperature have been varied. PH_3 pre-exposure has been also tested at low (550 °C) and high temperature (800 °C), for comparison.

2. Experimental

Epilayers of GaP were prepared using a horizontal AIX200/4 MOVPE reactor on Si(100) substrates with a 2° miscut toward the nearest (111) plane. Wafers were deoxidized using an HF dip and preheated at 800 °C in a H_2 flow for 30 min in order to remove any residual traces of silicon oxide and to promote the reconstruction of the surface. Before the GaP growth initiation, the substrates were exposed to two types of preflows (AsH_3 or PH_3) at low temperature (550 °C) or high temperature (800 °C). The GaP layer was grown in continuous mode by supplying TMGa and PH_3 as source materials at a V/III ratio of ~4000. The target layer thickness was 50 nm. The temperature for the pre-exposure step and for the subsequent GaP growth was the same. In Table 1, the pre-exposure conditions for each sample are summarized.

The crystalline structure of the layers was characterized using transmission electron microscopy (TEM). Samples were examined in a Philips Tecnai F20 operated at 200 kV. Samples were prepared in cross-section by standard sample preparation methods, mechanical

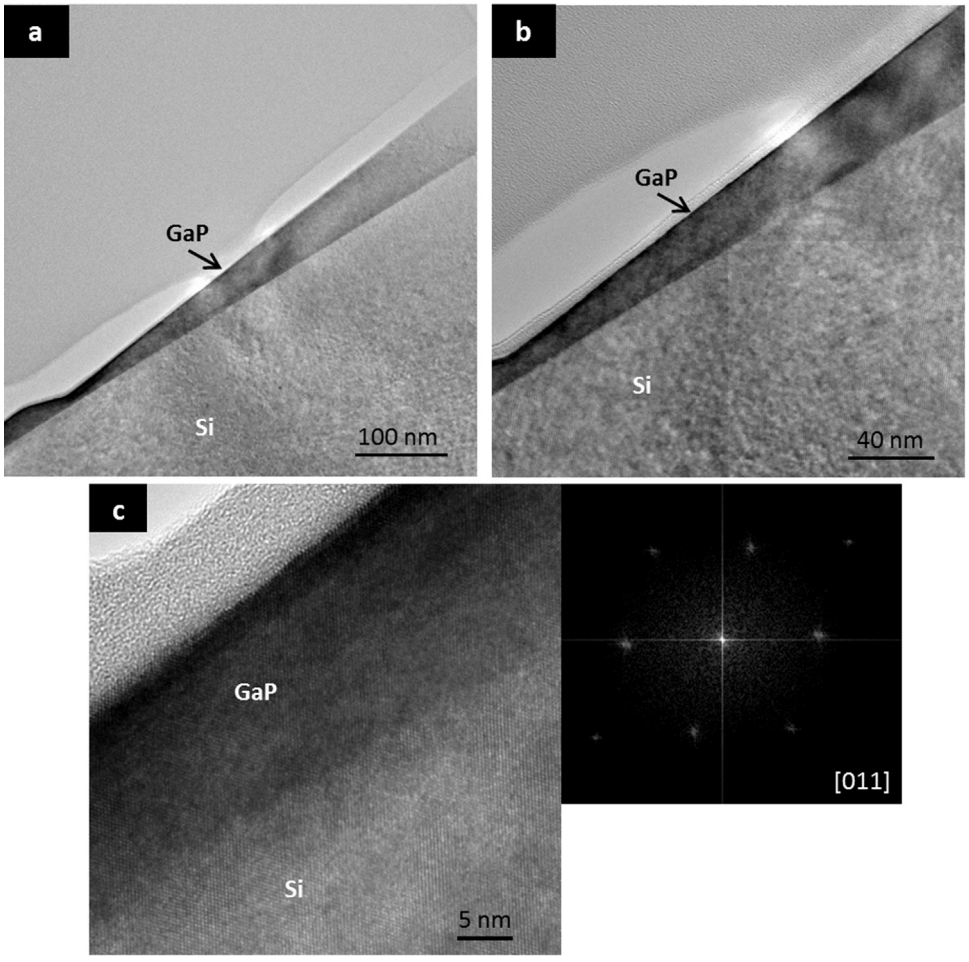

Fig. 1. Cross-sectional TEM images along the [011] direction of sample As-30s-800C (AsH_3 pre-exposure during 30 s at 800 °C). Fig. 1a and b show low resolution BF images. Fig. 1c shows HRTEM and FFT analysis.