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The effect of AlN nucleation temperature on inverted pyramid defects in GaN layers grown on 200 mm silicon wafers

Matthew Charles[a,b,*], Yannick Baines[a,b], Sandra Bos[a,b], René Escoffier[a,b], Gennie Garnier[a,b], Joël Kanyandekwe[a,b], Julie Lebreton[a,b], William Vandendaele[a]

[a] Univ. Grenoble Alpes, F-38000 Grenoble, France
[b] CEA, LETI, MINATEC Campus, F-38054 Grenoble, France

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ABSTRACT

We have examined 200 mm GaN on silicon wafers, while varying the AlN nucleation temperature, and have found that higher temperatures result in a more convex bow on the wafers. In addition, by performing full wafer defect mapping, we have found that a higher nucleation temperature results in a higher density of inverted pyramid defects, which have previously been found to reduce the breakdown voltage of GaN on silicon layers.

We have performed electrical measurements on a wafer with the lowest temperature AlN layer, which is still within our bow specification, and which therefore has the lowest density of inverted pyramid defects. This wafer showed the same leakage current density for both very small and very large test structures (2×10^{-3} and 18.7 mm^2 respectively), with all but one of our large structures maintaining a breakdown voltage greater than 700 V. This is a very promising result for high yield of devices on 200 mm GaN on silicon wafers.

1. Introduction

There is a great deal of interest in growth of gallium nitride (GaN) on silicon, in particular for applications in power electronics [1]. The interest of this type of substrate is that it becomes possible to use 200 mm wafers, and to access the high quality processing lines of CMOS fabrication plants. In order to ensure high yield on these devices, it is important to quantify and analyze the defects in the epitaxial layers which cause devices to fail, and find ways to solve these problems.

Growth of GaN on silicon cannot take place directly [2], due to reactions between gallium and silicon at the high growth temperatures used for GaN growth. This means that typically AlN layers are used as a nucleation layer [3,4], which also forms a barrier between the silicon and the gallium. In addition, the AlN has a smaller lattice parameter, which means that GaN grown on top will typically be under compressive strain. This enables the management of the strain in the buffer layers and GaN to ensure that the thermal expansion coefficient difference between GaN and silicon can be compensated, so that the wafer becomes flat after being cooled down from growth temperatures.

When analyzing critical defects in GaN layers, inverted pyramid defects, as shown in Fig. 1, have been shown to have a severe impact on the breakdown voltage of devices [5]. We have shown by electrical simulations [6] that the geometrical shape of these defects would be expected to increase the electric field at the bottom of the pit by a factor of 2–3 times, and this gives a first order explanation for the premature failure of test structures. It is therefore critical to control the density of these defects in order to achieve high device yield.

We have previously examined different nucleation conditions for AlN on silicon such as TMAl and NH_3 pre-injection before starting the growth. We examined the effect on the crystalline quality of GaN films grown on these nucleation layers and the relationship between this quality and the density of inverted pyramid defects [6]. The aim of the current study was to examine the effect of AlN nucleation layer temperature on the GaN layers grown on top, looking in particular at two aspects which are critical for processing large power devices in 200 mm cleanrooms: the wafer bow and the density of inverted pyramid defects.

2. Experimental method

The samples were grown by metal organic vapor phase epitaxy (MOVPE) using an AIXTRON Crius R200 single wafer close coupled showerhead tool. This tool includes an in-situ cleaning of the chamber using Cl_2 based gases, which occurs between every growth. The carrier gas was hydrogen for all layers, and the precursors for aluminum and gallium were tri-methyl aluminum (TMAl) and tri-methyl gallium (TMGa) respectively. Ammonia was used as the nitrogen precursor.

The temperature and bow were measured in-situ using a Laytec EpiCurve TT pyrometry and laser reflection system. The High

* Corresponding author at: CEA, LETI, MINATEC Campus, F-38054 Grenoble, France.

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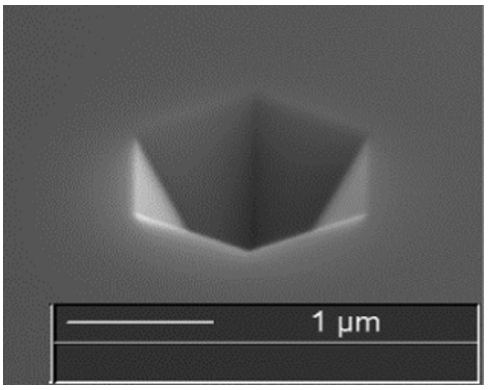

Fig. 1. SEM image of an inverted pyramid defect.

Resolution X-Ray Diffraction (HR-XRD) was performed using a Panalytical Xpert Pro tool, in triple axis mode, the bow was measured using an FRT Microprof system, and the defect detection was performed on an Applied Materials Complus 4T tool.

The 200 mm silicon (111) wafers were 1 mm thick, with orientation 0.2–0.3° miscut towards the (011) plane, and had a standard Radio Corporation of America (RCA) treatment before processing [7]. The wafers were annealed under hydrogen in the growth chamber for 4 min at 1040 °C in order to remove the native oxide and to prepare the silicon surface for growth.

The AlN layers were grown in two stages, firstly a nucleation layer of 50 nm at between 975 °C and 995 °C, followed by a second, 250 nm thick bulk layer of AlN at around 1100 °C. For the initial stages of the growth, other groups using MOVPE have introduced TMAl before NH_3 [8] or the two at the same time [9]. However, after using our Cl_2 cleaning of the growth, we have had better results using TMAl first [6], and this is the same growth scheme as has been used for MBE growth of AlN on silicon [10]. The AlN layers were grown at 100 mbar, with a V/III ratio of 330.

Following the AlN growth, an AlGaN based buffer 1.5 µm thick was grown at 75 mbar, followed by a GaN layer 1.8 µm thick, and AlGaN barrier layers less than 30 nm thick. The GaN layer was grown at 1040 °C, with reactor pressure of 100 mbar, using a V/III ratio of 560. The GaN layer growth conditions were chosen to be favorable to high carbon incorporation, as this has been shown to improve breakdown voltage of GaN structures [11]. The barrier layers had some variation between 20 nm and 30 nm thickness, and between 20% and 25% aluminum composition, as these wafers were designed for different resistance values. Otherwise the entire structure was nominally identical for all of these wafers. A schematic of these layers is shown in Fig. 2.

For the electrical test structures, round mesa structures, with a height of around 250 nm were created across an entire 200 mm wafer, with the top of each mesa coated with metal. Their diameter varied from 50 µm to 4.8 mm. This allowed vertical I-V measurements to be made, in order to find the breakdown voltage, and the leakage current at 600 V.

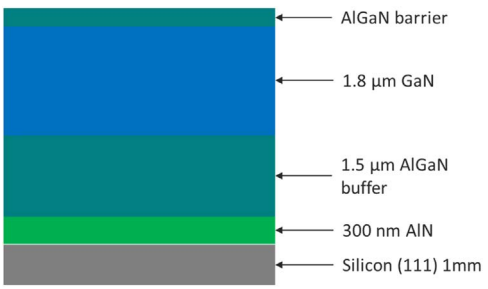

Fig. 2. Schematic of the GaN based structures grown on silicon.

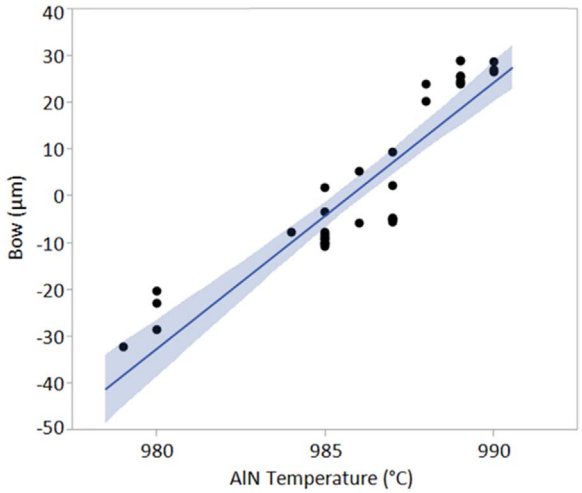

Fig. 3. Wafer bow plotted against AlN nucleation temperature, with a positive bow representing a convex wafer, and a negative bow a concave wafer.

3. Results and discussion

The first measurements compared the wafer bow with the AlN nucleation temperature, as shown in Fig. 3, with a very clear correlation between the two. Although not shown here, it should be noted that all wafers were crack free except for a narrow edge exclusion area. The graph shows that the bow is very sensitive to the AlN nucleation temperature, with the wafer bow changing from +30 µm (convex) to −30 µm (concave) with a reduction in the nucleation layer temperature of just over 10 °C.

This result may be better understood by examining two correlations which have been found on a smaller set of samples, as shown in Fig. 4. Again, the samples are identical apart from changes to the AlN nucleation layer. There is a clear correlation between the wafer bow and the full width at half maximum (FWHM) of the GaN (101) reflection, with a more positive bow for narrower peak widths. Equally, the strain in the GaN film, calculated from the c-parameter of GaN as measured by XRD of the (002) reflection, is less tensile for narrower peak widths. This can be explained by a mechanism of relaxation by annihilation of edge type dislocations. When there is a higher edge type dislocation density and therefore a larger (101) peak width, the dislocations can annihilate more easily because the average distance between them is reduced. When an annihilation occurs, the film relaxes, reducing the compressive strain at growth temperature. This translates to an increased tensile strain once the wafer has been cooled to room temperature from the growth temperature of 1040 °C

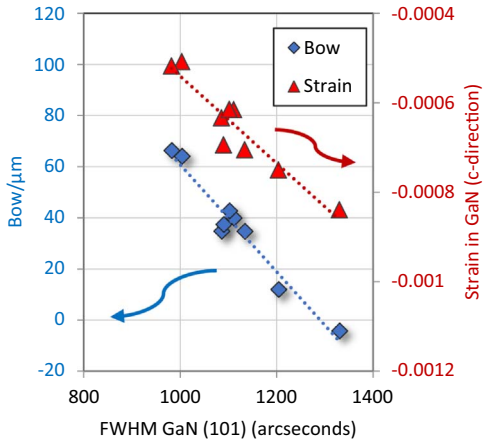

Fig. 4. Wafer bow (blue diamonds) and GaN strain (red triangles) plotted against the FWHM of the GaN (101) peak.