

# Generation mechanism of large-size invisible defects on Si epitaxial wafers



Kyuhyung Lee\*, Jungkil Park, Jungwon Shin, Jayoung Kim, Heebog Kang, Boyoung Lee

Research Center, LG Siltron Inc., Gumi-si, Gyeongsangbuk-do 730-350, Korea

## ARTICLE INFO

Communicated by T.F. Kuech

Keywords:

A1. Defects

A1. Etching

A3. Chemical vapor deposition processes

B2. Semiconducting silicon

## ABSTRACT

The new Si epitaxial (epi) defects not seen in scanning electron microscope (SEM) measurements were investigated. Morphologies of these defects were measured by atomic force microscope (AFM) but source of defect was not found in transmission electron microscope (TEM) measurements. In order to find the origin of the invisible defect, we observed the morphological changes of the various substrate defects after epi growth process. Most of the defects were removed during hydrogen (H<sub>2</sub>) baking and hydrogen chloride (HCl) etching steps, but some particles survived. Among the survived defects, it was confirmed that the non-metallic particles having 200 nm or more were the origin of the invisible epi defects.

## 1. Introduction

Silicon wafers have been predominantly used for large-scale integrated (LSI) memory device fabrication. It is well known that Czochralski (CZ) grown-in defects on the polished wafer surface cause device failures, such as gate oxide breakdown and leakage current of p–n junction [1–3]. Besides grown-in defects, various surface or near-surface defects such as polishing induced defect (PID) and metal-induced defect (MID) affect the performance of the semiconductor device or device yield [4–6]. Since silicon wafer with epitaxially grown layer can control not only the surface defects but also the doping profile, it can improve quite effectively the device performance [7,8]. Thus the use of epi wafer has been gradually increasing not only for micro-processor but also for complementary metal–oxide–semiconductor (CMOS) image sensor. Even in epi wafer, however, there still exist specific epi defects and these defects can also cause deterioration of the chip performance or failure [9,10]. In order to control these defects, it is important to understand the sources and generation mechanisms of epi defects.

Epi defects are generated by various sources such as substrate particle, thermal stress, and lattice mismatch between substrate and epi layer. Since common epi defects such as epi stacking fault (ESF), thermal slip, and misfit dislocation are already known source or generation mechanism, these known defects can be relatively easily controlled [11]. As the design rule of the semiconductor device continues to shrink, the requirements of the wafer also continue to be stringent. Therefore, new defects not previously classified as defects are occasionally occurred. To control the newly defined defects, we must confirm the actual shape of the defect and understand the

generation mechanism. However, it is hard to control the defects since some defects are occasionally difficult to observe the actual shape due to the limitation of the equipment performance.

In this paper, we observed the new epi defects not seen in SEM measurements and investigated the origin of the defects. And we proposed the generation mechanism of these invisible epi defects.

## 2. Experimental

We prepared two groups of wafers. One group was lightly boron-doped (100) CZ-Si substrate with a diameter of 300 mm and substrate resistivities of 20–25 Ω·cm ([B]=5.34E14–6.67E14 cm<sup>-3</sup>). Another group was heavily boron-doped (100) CZ-Si substrate with a 300 mm and resistivities of 7–10 mΩ·cm ([B]=8.49E18–1.34E19 cm<sup>-3</sup>). Substrate was loaded in the reaction chamber under H<sub>2</sub> gas condition so as to remove the native oxide at high temperature above 1100 °C for 60 s with 20slm. Then, HCl gas was flowed to etch the silicon surface in order to remove surface damage or defects prior to Si epi growth. HCl etch gas was flowed at 1150 °C for 120 s with 0.5slm. Etched depth of the substrate was approximately 200 nm. Finally, Si epi growth process using trichlorosilane (SiHCl<sub>3</sub>, TCS) was carried out. Epi growth processes were progressed at high temperature above 1100 °C. The thickness of the epi layer was approximately 2 μm.

Two kinds of experiments were carried out. First experiment was performed to confirm the actual shape of the invisible defect after epi growth. After epi growth, we performed defect inspection using particle counter (KLA-tencor) and followed by SEM (Hitachi High-Technologies corporation) measurements. And then, invisible epi defects in SEM measurements were reviewed and marked the position

\* Corresponding author.

E-mail address: [kyuhyung.lee@lgsiltron.co.kr](mailto:kyuhyung.lee@lgsiltron.co.kr) (K. Lee).

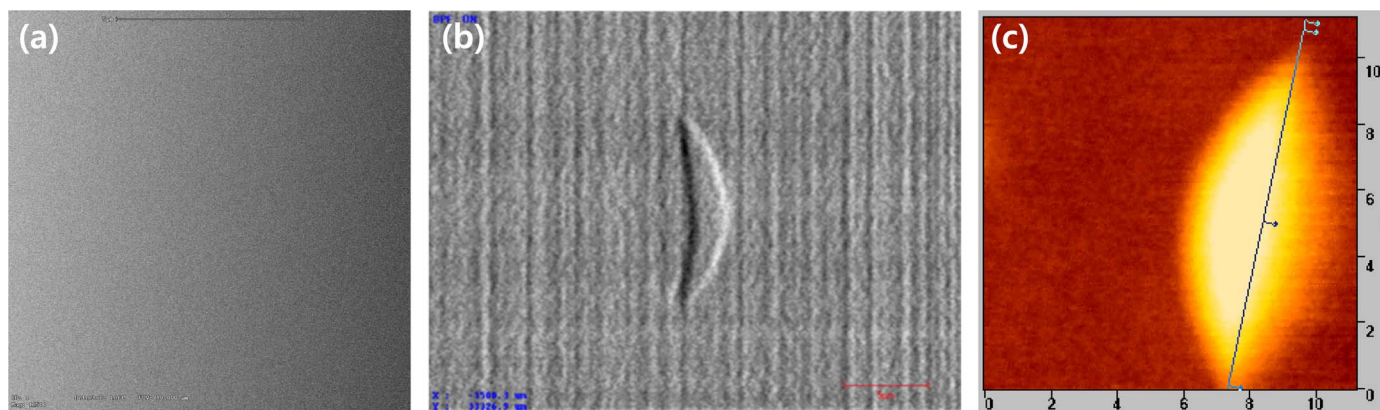


Fig. 1. Same epi defect images of (a) SEM, (b) MAGICS, and (c) AFM.

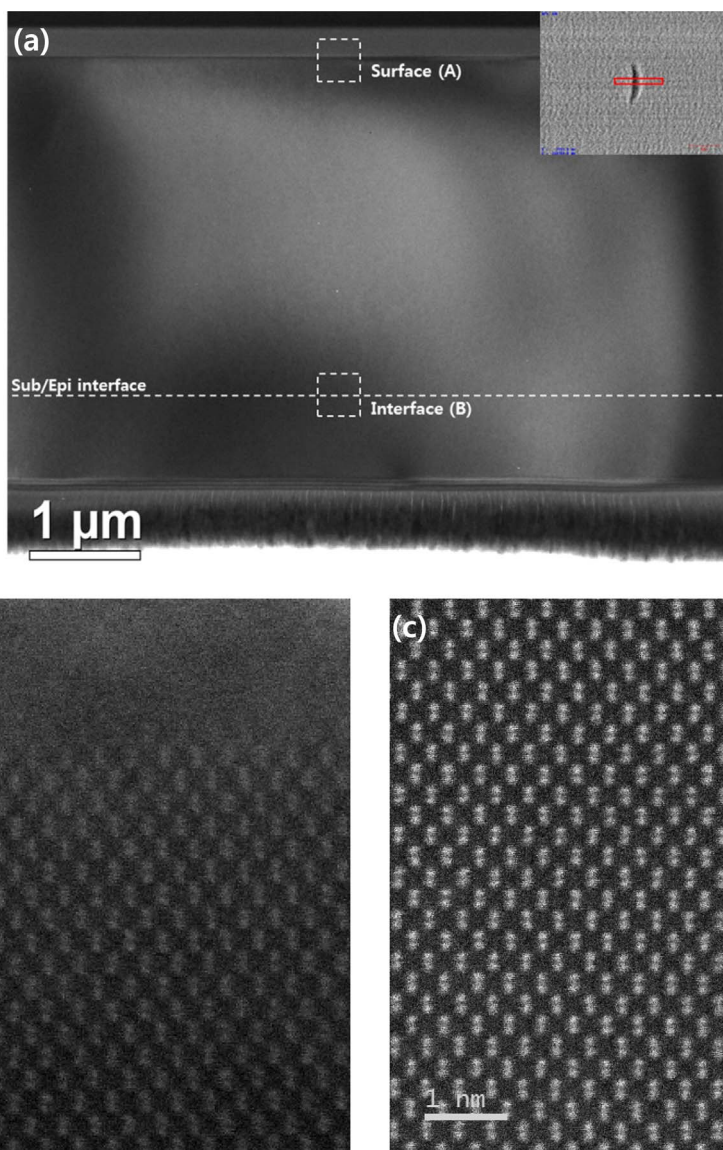


Fig. 2. Cross-sectional TEM images of invisible epi defect: (a) Low magnification bright-field TEM and HR-STEM images of (b) the surface and (c) heavily boron-doped substrate/epi layer interface region of the defects. Inset of (a) shows the defect image of the MAGICS tool and red rectangle region indicates position of the cross-sectional TEM sampling. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

using multiple image acquisition for giga-bit pattern inspection with confocal System (MAGICS, Lasertec corporation). Subsequently, AFM (Seiko Instruments) and TEM (FEI and JEOL) measurements were conducted to obtain morphology and size of the defects. The samples

for the cross-sectional TEM measurements were prepared by cutting and ion milling using dual-beam focused ion beam (DB-FIB, FEI).

Second experiment was performed to identify the defect source transformed into the invisible defect after epi growth. In order to find

Download English Version:

<https://daneshyari.com/en/article/5489475>

Download Persian Version:

<https://daneshyari.com/article/5489475>

[Daneshyari.com](https://daneshyari.com)