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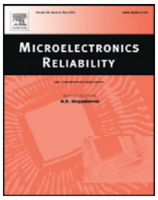

Adhesion energy of printed circuit board materials using four-point-bending validated with finite element simulations

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ABSTRACT

Modern printed circuit boards (PCB) are high performance products consisting of metal and dielectric materials in a multi-layered structure. Due to this build-up different failures, such as cracking or delamination, may occur during manufacturing and use leading to failure of the entire electronic device. The mismatch in the thermal expansion coefficients leads to stresses in the structure during temperature change, e.g., during the reflow process. To improve device reliability, it is critical to understand the delamination between different layers and to know the adhesion energy of the interfaces in a PCB. The adhesion energy in test PCBs was determined using four point bending (4PB) experiments before and after 15 reflow cycles. The investigations show that 4PB is applicable for determining the adhesion energy in samples made of halogen free pre-pregs and copper sheets with standard manufacturing processes. Furthermore, the applicability of the analytical adhesion energy calculation in the presence of non-linearities was examined by finite element simulations. It was found that friction between the sample and the pins of the loading device has an influence on the reaction force used for the calculation of the critical energy release rate. Plastic deformation of the 4PB sample, especially in the ductile copper layers, also will affect the analytically determined critical energy release rate. The role of both factors on the analytical approach to measure adhesion energies of PCB interfaces with 4PB will be shown and discussed.

1. Introduction

Early printed circuit boards (PCBs) were made of polymer panels onto which the electronic components were assembled using surface-mounted technology. The electrical connections were realized with copper traces plated or printed onto the surface of the panels. In order to overcome design limitations, multi-layer PCBs were manufactured, which allowed distributing the traces over multiple layers [1,2]. Intralayer connections were fabricated using copper-plated through-holes, the so-called vias. This new process lifted design limitations considerably, allowing for more complex and powerful boards to be realized, but also giving rise to new failure mechanisms. Due to the multi-layer build-up of different materials, e.g., copper and polymers with glass fiber reinforcement, cracking in the dielectric and/or delamination at dielectric-copper interfaces may occur during manufacturing and application of PCBs [3]. Typical weak points are the interface between the dielectric material (pre-preg made of a polymer composite) and the copper traces. They are often observed to fail during the reflow process which is used to mount components on PCBs with solders. To ensure stability of PCBs against reflow loading, the Moisture/Reflow Sensitivity test (IPC/JEDEC J-STD-020D.1) [4] is used. It is an integral part of the qualification procedure of new PCB designs and can be used to determine thermal reliability. During reflow the PCB is quickly heated up to 260 °C, the temperature at which the solder melts, followed by a cooling phase. Due to different elastic properties and coefficients of thermal expansion (CTE) stresses are introduced during the process which can lead to delaminations at the copper-dielectric interface.

Interface delaminations are driven by three main mechanisms: thermal mismatch between the different materials, swelling and degradation due to moisture absorption, and degradation due to thermal cycling [5–15]. In order to understand the delamination mechanism during thermal cycling the adhesion energy (also called critical energy release rate which can be expressed by the interfacial toughness) between copper and dielectric pre-preg needs to be known. At this point it should be noted that there is a subtle difference between energy release rate and toughness. The toughness is a property of the system whereas the energy release rate is the energy available in the system; at failure, the energy release rate of the system reaches its critical value that equals the toughness as a system property characterizing failure. Several techniques are available for quantifying the adhesion energy of interfaces, for example 3- and 4-point bending [16–21], scratch testing [21], spontaneous delamination due to compressive stresses [21–24], indentation induced delamination [21,25–27], and tensile

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straining induced delamination on compliant substrates [28,29]. These methods are all based on mechanical or thermo-mechanical theories and have been successfully applied to a variety of interfaces [16–29]. Of the mentioned techniques, 4-point bending (4PB) was found to be suitable to determine the steady state energy release rate (adhesion energy) between different kinds of metal–dielectric interfaces [30–34]. The 4PB test is highly valuable for studying multilayer systems because the interfaces of interest are sandwiched between two elastic substrates. The critical energy release rate of the interface is evaluated from load–displacement data using the sample dimensions, elastic properties of the substrates (normally silicon) and the average load plateau after failure. During the load plateau the interface crack is assumed to be opening under steady-state conditions. The determination of the critical energy release rate is based on the Euler–Bernoulli beam theory [35] and assumes linear elastic deformation behavior. Up to now, it is not clear whether the available analytical approaches are applicable to determine the critical energy release rate in the presence of non-linearities, such as plastic deformation within the layers or friction [30]. Therefore, Finite Element (FE) simulations are used to investigate these influences in a special PCB 4PB build-up which utilizes thick cores as the elastic substrates.

2. Experimental details

2.1. Specimen description

To ensure the relevance of the results for commercially produced PCBs, the 4PB samples with a pre-notch were produced using the same materials, fabrication methods and equipment that are used in commercial PCB production. To produce a test coupon optimized for 4PB tests two pressing cycles were utilized. The samples were built up from two continuous Cu foil (20 μm each thick) sided pre-pregs (360 μm thick), so-called cores, with a layer of pre-preg (85 μm) and continuous Cu foil (20 μm thick) on both sides and a pre-preg layer in the middle, see Fig. 1a. The first pressing step creates the elastic substrates (core plus pre-preg layer with Cu) and the second pressing step creates the interface of interest, namely the interface between the Cu and the pre-preg. During both pressing cycles the following production steps were used: the copper foils were chemically processed using industrial pre-treatments to increase the surface roughness on one side, followed by a coating with special binding agents. Afterwards standard lay-up and lamination procedures were utilized to laminate the copper foils and pre-pregs together at 180–200 °C under a pressure of 2–3 MPa to build the elastic substrate for the 4PB samples (in Fig. 1a, parts h_d and h_2). In the second pressing step two boards from the first pressing cycle were combined with another layer of pre-preg (75 μm thick) which was located in the middle of the sample (Fig. 1a, part h_1). Again, the Cu surfaces were chemically processed the same way as during the first pressing step, followed by the manual lay-up and laminating procedure at the same temperature and pressure. From the completed board, bending beams approximately 7 mm wide, 40 mm long and 1.3 mm thick were machined, see Fig. 1a and b. Notches in the beams were introduced by mechanically cutting through the top surface of the 4PB PCB samples with a router. The average notch depth was about 300 μm. After notching, half of the 4PB PCB cards were reflow cycled using the Moisture/Reflow Sensitivity test (IPC/JEDEC J-STD-020D.1) [4] by heating the cards to 260 °C in about 275 s followed by cooling down to 50 °C in about 125 s. To evaluate the influence of reflow cycles on adhesion of the Cu/pre-preg interface, 15 cycles were performed. The 15× reflowed samples were compared to samples that were not reflowed

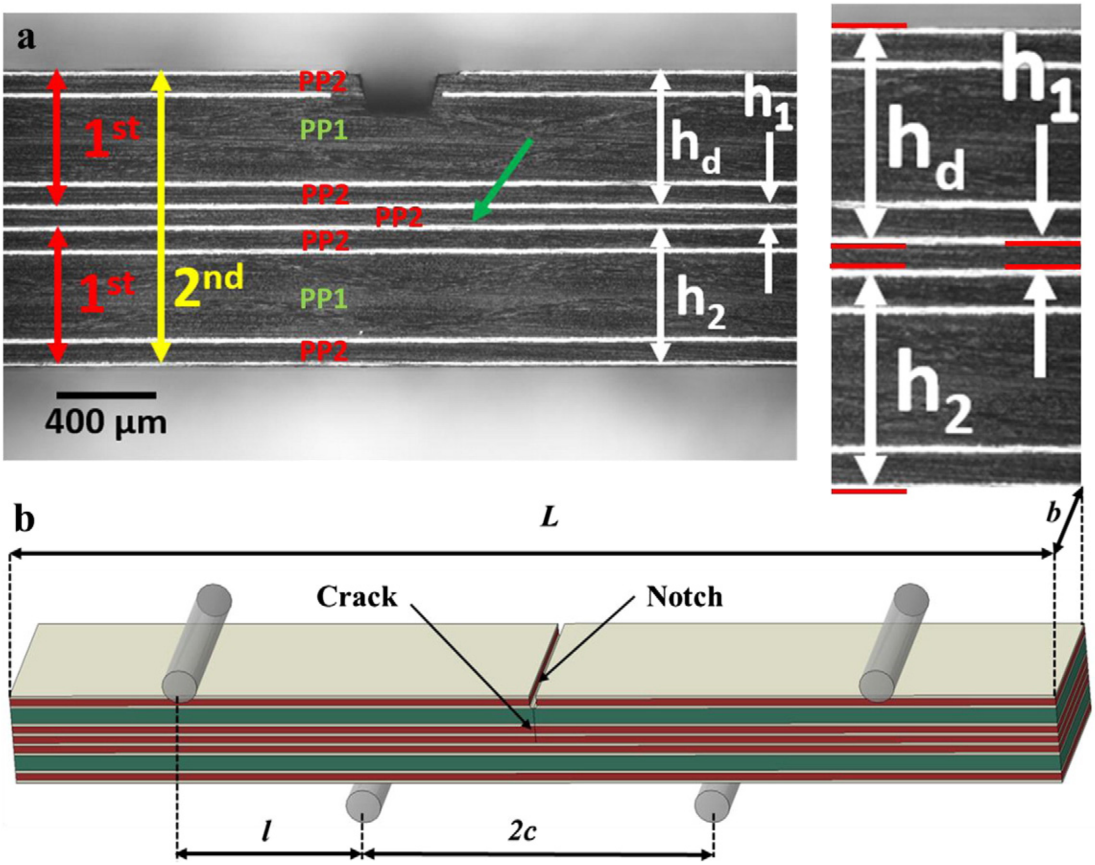

Fig. 1. (a) Cross section of the 4PB PCB build-up. Layers of Pre-preg 1 and Pre-preg 2 are indicated as PP1 and PP2, respectively. The red arrow shows the laminate after the first pressing cycle, the yellow arrow indicates the final sample after the second pressing cycle. The green arrow indicates the critical interface of interest. (b) Schematic diagram of the test set-up with a notched multi-layer bending sample.