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Influence of vertical temperature gradients on wafer quality and cell efficiency of Seed-assisted high-performance multi-crystalline silicon

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ABSTRACT

The effect of vertical temperature gradients on the performance of Seed-assisted high-performance (HP) multi-crystalline silicon (mc-Si) is investigated by numerical simulations and contrast experiments. The vertical temperature gradients are designed by keeping the temperatures at the top and lowering the temperatures at the bottom. Two Seed-assisted HP mc-Si ingots were grown by means of a larger and a conventional vertical temperature gradient. It is found that the larger vertical temperature gradients result in the more parallel growth direction of grains and the longer crystal growth length, increases the percentages of <112> grain orientation and random grain boundaries, which are benefit for crystal quality. The experimental results also confirm that the wafer of ingot grown with a larger vertical gradient has the better quality, and their cell efficiency can increase.

Keywords:
Multi-crystalline silicon, Seed-assisted HP, Temperature gradient, Grain orientation, Grain boundary, Wafer quality, Cell efficiency

1. Introduction

The recent development of the so-called seed-assisted HP mc-Si based on the nucleation of small grains with dominant non-coherent grain boundaries has attracted much attention in industry [1-5]. The most common way to obtain small grains is to use silicon particles as seeds. A layer of special silicon feedstock material is typically placed on the crucible bottom, which is partially melted during the initial phase of the