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# Sintered silver finite element modelling and reliability based design optimisation in power electronic module

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ABSTRACT

This paper discusses the design for reliability of a sintered silver structure in a power electronic module based on the computational approach that composed of high fidelity analysis, reduced order modelling, numerical risk analysis, and optimisation. The methodology was demonstrated on sintered silver interconnect sandwiched between silicon carbide chip and copper substrate in a power electronic module. In particular, sintered silver reliability due to thermal fatigue material degradation is one of the main concerns. Thermo-mechanical behaviour of the power module sintered silver joint structure is simulated by finite element analysis for cyclic temperature loading profile in order to capture the strain distribution. The discussion was on methods for approximate reduced order modelling based on interpolation techniques using Kriging and radial basis functions. The reduced order modelling approach uses prediction data for the thermo-mechanical behaviour. The fatigue lifetime of the sintered silver interconnect and the warpage of the interconnect layer was particular interest in this study. The reduced order models were used for the analysis of the effect of design uncertainties on the reliability of the sintered silver layer. To assess the effect of uncertain design data, a method for estimating the variation of reliability related metrics namely Latin Hypercube sampling was utilised. The product capability indices are evaluated from the distributions fitted to the histogram resulting from Latin Hypercube sampling technique. A reliability based design optimisation was demonstrated using Particle Swarm Optimisation algorithm for constraint optimisation task consists of optimising two different characteristic performance metrics such as the thermo-mechanical plastic strain accumulation per cycle on the sintered layer and the thermally induced warpage.

## 1. Introduction

In a power electronic module, the silicon chip is attached by die attach materials usually solder materials to package substrate material. The package substrate is typically composed of ceramic isolated by copper layers. Nowadays silicon chips are replaced by silicon carbide chips which is able to withstand a temperature up to 500 °C [1]. However die attach materials such as solders cannot endure a temperature of above 200 °C. Lead free solders such as SnAgCu has the melting temperature of 220 °C. These lead free solders can be used as die attach material for up to 80% of the melting temperature before creep strain effects cause failure [1]. To enhance the thermo mechanical behaviour of die attach material, one of the approach is to use the sintered silver joint as die attach. Sintered silver joint has a high melting temperature, together with silicon carbide die is more suitable combination for high temperature application of power electronic module. The limitation of successful application of sintered silver interconnect is its long term reliability depends on the density of the sintered layer, types of substrates, substrate roughness, joint configuration (die sizes and interconnect thickness) formulation of sintered silver paste and other factors [2].

Experimental observations of power module with thin sintered silver layer (20 μm) as die attach material subject to thermal cyclic loading are listed below from the study by Herboth et al. [3]

- Cracks initiated and propagated into interconnected network cracks.
- Cracks penetrated through the sintered Ag layer nearly vertically.

The observation concluded that primary failure mechanism of sintered layer was due to deformation by plasticity and the fracture mechanism in the sintered layer was intergranular fracture caused by the grain boundary porosity [3]. This observation

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motivated us to conduct a finite element analysis on sintered silver structural model in the hope of replicating these observations. Additionally this study is concluded with a reliability based design optimisation on sintered silver structure. Herboth's experimental observation in [3] was in contrast to the experimental observation discussed by DeVoto et al. [4]. In DeVoto's article, it was reported that experimental observation of perimeter delamination of sintered silver layer as function of number of thermal cycles.

A review of the finite element modelling of sintered silver joint in power module applications are discussed in this paragraph. A 2D finite element modelling of sintered silver structure using Anand visco-plastic constitutive model to simulate the inelastic strain deformation is discussed by Chen et al. [5]. Chen's article concluded that under thermal cycling conditions a ratcheting effect [6] of shear stress and strain in the sintered silver joint attached to chip. Another 2D FEA study on sintered silver structure for residual bending was simulated by Mei et al. [7]. A simplified relationship for residual curvature versus joint size was also proposed with number of assumptions and FEA result was compared with experimental results [7]. In Herboth's article [3] a 3D FEA was conducted using a linear elastic fracture mechanics based crack initiation and propagation model and concluded that maximum stress intensity is related to diameter of the sintered silver joint for same substrate size. Another Herboth article [8] discusses a FEA on sintered layer structure and concluded that the cracks initiate at the edges of the die/sintered layer interface. Bai et al. [9] simulated 3D FEA on sintered silver attached to silicon carbide chip and observed that thermo mechanical stresses are high on the perimeter of the interface.

## 2. Finite element analysis of sintered silver in power module

In this section, the method and results of using finite element analysis computer modelling to investigate the effect of varying thermal load on the residual stress in the sintered silver layer are presented. To simulate the thermo mechanical loading condition on a sintered silver structure in Ansys FEA software [10] we generated the three dimensional finite element models as shown in Fig. 1, Dimensions of the structure are indicated in Fig. 1.

The length and width of the silicon carbide chip is 2.5 mm × 2.5 mm and the silicon nitride length and width are chosen as 7.5 mm × 7.5 mm. The elastic and thermal material properties of all the materials used in this model are listed in Table 1 and plastic material properties are listed in Table 2. The material properties of sintered silver interconnect were obtained from the thesis by Bai [11]. Additional sintered silver material properties are extracted from the technical report by Wereszczak et al. [12]. Fig. 1 shows geometry and materials of the different layers. According to Dudek et al. [13] the sintered silver shows elastic–plastic behaviour without the strong creep of soft solder up to the high temperature range (150 °C). Additionally Chen et al. [6] concluded from their experiment that the process of damage evolution of sintered silver interconnects was temperature independent. Hence we utilised elastic–plastic behaviour of the sinter layer instead of creep characteristic. Beside, creep data for the sintered layer was unavailable at the time of the study. In this study, FEA simulations in Ansys were a passive thermo mechanical analysis using the element SOLID185. The parts in the model associated with critical regions of interest have finer mesh in order to ensure accurate FEA results.

**Table 1**
Elastic and thermal material properties used in the FEA.

| Properties | Silicon Carbide (SiC) | Silicon Nitrate ($Si_3N_4$) | Copper (Cu) | Sintered Silver (80% dense) | Pure Silver |
|---|---|---|---|---|---|
| Thermal conductivity (W/(K m)) | 370 | 70 | 401 | 240 | 430 |
| Specific heat (J/(kg °C) | 750 | 691 | 390 | 234 | 234 |
| Density (kg/cm$^3$) | 3.21 | 2.40 | 8.96 | 8.4 | 10.492 |
| Coefficient of thermal expansion ($10^{-6}$/K) | 4.0 | 3.0 | 16.5 | 19 | 18.9 |
| Young's modulus (GPa) | 410 | 314 | 128 | 10 | 83.5 |
| Poisson ratio | 0.14 | 0.3 | 0.34 | 0.37 | 0.37 |

**Table 2**
Plastic material property used in the FEA.

| | Sintered silver (80% dense) | Pure silver |
|---|---|---|
| Yield strength (MPa) | 43 | 55 |
| Tangent modulus (MPa) | 0 | 133 |

The three point movement restraining boundary condition were imposed on the model. All three degrees of freedom at a lower point are fixed and then two degrees of freedom of the next lower point is fixed and one degree of freedom of the third lower point is fixed. Temperature cyclic loading as in Fig. 2(b) is imposed on a passive thermo-mechanical analysis. Due to convergence issue with iterative solver in Ansys mechanical software, we utilised discreet static analysis using LOAD STEP option in all finite element simulations. The output extracted from the finite element simulation are accumulated plastic strain as in Fig. 3 and relative displacement as in Fig. 4. In Fig. 4, the point A is the upper middle point of the sintered silver layer and point B is the lower middle point of the sintered layer. Relative displacement between point A and B is defined as

$$D_R = \sqrt{(u_A - u_B)^2 + (v_A - v_B)^2 + (w_A - w_B)^2}$$

The evaluation of predictive fatigue lifetime of solder joint can be categorised based on stress, plastic strain, plastic and creep strain, energy, and damage accumulation during a test [14]. For sintered silver interconnect with elasto plastic material properties we used a plastic strain based life prediction model which only considers plastic phenomena caused by coefficient of thermal

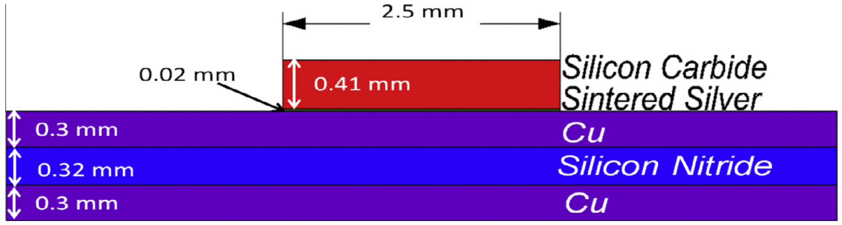

**Fig. 1.** The dimensions of the sintered silver finite element model.