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Impact of substrate resistance and layout on passivation etch-induced wafer arcing and reliability

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ABSTRACT

Wafer arcing, as a form of plasma-induced damage, occurs randomly, varies among different products and introduces problems into production yield and reliability. Conventional arcing theory is based on substrate conductive paths, for which the arcing frequency decreases as the substrate resistance increases. However, we observed the reverse result, i.e., silicon-on-insulator (SOI) and integrated passive device (IPD) wafers with high substrate resistance suffered a high frequency of passivation (PA) etch-induced arcing. In addition, the newly developed through silicon vias (TSV) interposer process for three-dimensional (3D) packaging also encountered a similar problem. To explain and solve these problems, we used substrates of different resistivities using the arcing-enhanced method to study this PA etch-induced wafer arcing phenomenon and revealed the mechanism underlying the effect of substrate resistance, the role of the seal ring, the root cause of the layout's effect on arcing frequency and the impact on reliability. Next, we determined that the reduction in arcing relies on the simultaneous optimization of the process and the layout and observed that the reduction of the arcing source helps to improve product reliability. Finally, improvement methods and guidelines were proposed for both the process and the layout.

1. Introduction

Wafer arcing is a phenomenon of strong discharge that occurs during plasma processes, such as implantation [1], high-density plasma (HDP) dielectric deposition [2], contact, metal, via, and passivation (PA) etching [3,4]. Among these processes, PA etching causes the highest arcing frequency (the ratio between the number of arcing wafers and the number of total processed wafers) due to its high RF power and the presence of the most complex underlying layers. In contrast to traditional plasma-induced damage (PID), which leads to shifts in the electrical parameters of devices [5,6], wafer arcing causes dielectric rupture and conductor burnout and is directly observable under examination via scanning electron microscopy (SEM), X-ray diffraction [7] or strong light [8], resulting in large yield loss and reliability failure simultaneously.

A comprehensive and widely accepted wafer arcing mechanism was presented by Ma et al. [9]. As shown in Fig. 1, an unstable plasma causes a horizontal DC voltage drop on the wafer, which discharges through a closed conductive path and results in wafer arcing. According to this mechanism, the arcing frequency should decrease with increasing substrate resistivity. However, our statistical data demonstrated the opposite results: the PA etch-induced arcing frequencies of 10-Ω cm (standard radio frequency CMOS, RF-CMOS, bulk silicon), 100-Ω cm (high-performance RF-CMOS, bulk silicon) and 600-Ω cm (SOI wafer, the thickness of silicon on the insulator is 2000 Å; 600 Ω cm is the result of being converted to the standard 720-μm bulk silicon) substrates were 0.004%, 0.02% and 0.5% respectively. The arcing frequency of an SOI wafer was reduced to 0.03% by optimizing the PA etching process. However, for an integrated passive device (IPD) product with a 1000-Ω cm substrate, which has become popular in recent years under the requirement of high-performance passive devices for RF applications [10], the PA etch-induced arcing frequency was as high as 1%; optimizing the process did help but did not solve this problem. At the same time, the newly developed through silicon vias (TSV) interposer process for 3D packaging also suffered a similar problem, which greatly affected product yield and quality.

Similar to substrate resistance, wafer arcing also exhibits a strong correlation with the seal ring and layout, such as the power bus design, based on our observations. Consequently, this substrate resistance, seal ring and layout-dependent arcing

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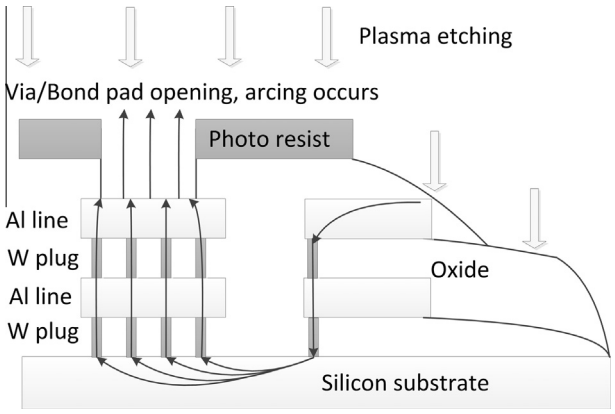

Fig. 1. Conventional wafer arcing mechanism [9] in which charge is collected from an exposed metal or tungsten plug residues at the wafer edge and propagates through the substrate into the bond pad; subsequently, arcing occurs during pad or via etching.

mechanism, along with the impact on the reliability of the arcing and methods for reducing the arcing, were studied in this work.

2. Experimental

Because the wafer arcing frequency is very low [9] and difficult to study, the occurrence of wafer arcing must first be enhanced. Wafer edge exposure (WEE) is one important process for preventing arcing by removing metal residues at the wafer edge; to enhance the arcing frequency, we reversed the standard 0.18-μm CMOS WEE rules and set the metal/PA WEE to be 1.0-/2.8-mm, thus intentionally exposing the wafer edge metal to PA etching. At the same time, the RF power of the PA etching process was increased to introduce a higher arcing frequency as well.

In addition to the above-described process, the seal ring is another important factor because arcing is always accompanied by the burnout of a seal ring. To determine the role of the seal ring in arcing, we designed experiments involving cases with versus without seal rings and using closed versus unclosed seal rings for the same chip. Furthermore, to verify the conventional arcing mechanism, every wafer with four chips remained unexposed to PA photoresist; consequently, no bond pads were exposed to the PA etching process, and no arcing should have occurred, according to [9].

Subsequently, the standard 200-mm 0.18-μm RF-CMOS process was conducted on nine pieces of 10-Ω cm p-type bulk silicon, 100-Ω cm p-type bulk silicon, 600-Ω cm SOI wafer, and 1000-Ω cm (IPD process) p-type substrates with the same back end of line (BEOL) processes. Each of the first three types of substrate originated from the front end of line (FEOL) process, and the IPD wafers originated from the BEOL metal process directly after interlayer dielectric (ILD) deposition. Due to the lack of contact processes, all IPD metals were floated by an ILD, and the substrate resistance became infinite during PA etching.

3. Results and discussions

3.1. Arcing results

Wafer arcing occurred during PA etching and was then investigated, analyzed and verified. For all 27 pieces, the wafer was started from the FEOL with reversed WEE rules, and only one SOI wafer was observed to have a minor arcing point at the wafer edge. Meanwhile, among the IPD experimental wafers with an infinite substrate resistance and wafer edge-exposed metal, four of nine were observed to exhibit serious arcing.

Fig. 2 shows images and arcing footprints of the initial-to-serious arcing points observed on the IPD wafer. Arcing initiated from the wafer edge (pattern c in Fig. 2), propagated through the metal lines of the seal ring (patterns c and f in Fig. 2), and then occurred extensively in the wafer center (patterns d and g in Fig. 2). At the same time, we observed that arcing occurred only in the area with a seal ring and not in the area from which the seal ring was removed; arcing also occurred more extensively in the closed seal ring and much less extensively in the unclosed seal ring areas. For

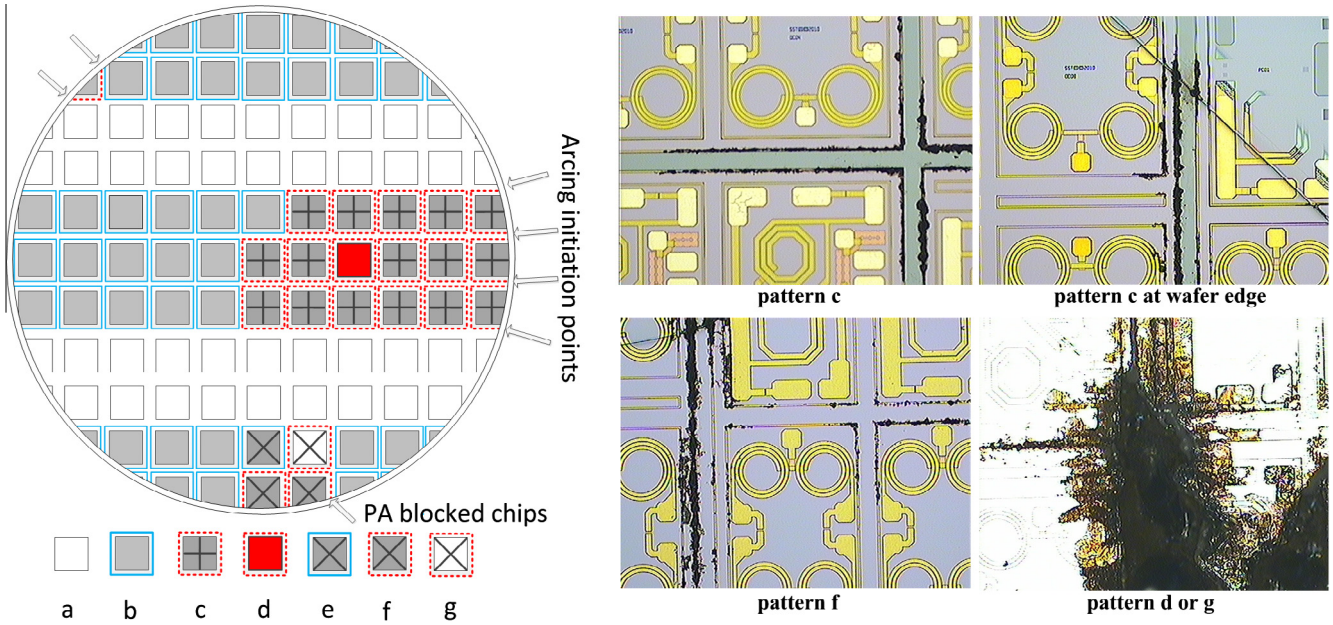

Fig. 2. Arcing footprints and images of the IPD wafer: pattern a. chip without a seal ring; pattern b. chip with a seal ring; pattern c. chip with a burned out seal ring; pattern d. chip with a burned out seal ring and extensive arcing; pattern e. chip with PA etching blocked; pattern f. chip with PA etching blocked and with a burned out seal ring; pattern g. chip with PA etching blocked and with a burned out seal ring and extensive arcing. Images showing the typical effects of arcing on patterns c, f, d, and g are shown on the right.