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Screening small-delay defects using inter-path correlation to reduce reliability risk

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ABSTRACT

Subtle defects such as low resistive vias and high resistive shorts cause Small-Delay Defects that are hard to detect even by advanced test methodologies. Detection of these defects aggravates with process variations becoming an important source of test escapes. Furthermore, these defects may degrade with time posing a reliability risk. In this paper, a novel methodology to detect SDDs in the presence of process variations using delay correlation information between logic paths of a circuit is proposed. This methodology exploits the concept that for two correlated paths, a part of the delay variance in one path can be described by the delay variance in other path. Using multiple path prediction allows to further improve the detection of SDDs. A path-based statistical timing analysis framework has been developed and implemented to compute timing information and inter-path correlation. Spatial and structural correlation, and random dopant fluctuations are considered. Simulation results in ISCAS85 benchmark circuits show that the proposed methodology is able to detect SDDs in the slack interval and to distinguish delay defects from process variations. The obtained results give indication of the promising capabilities of the proposed technique to detect "very" small-delay defects. Hence, test quality is improved leading to higher product reliability.

1. Introduction

Subtle defects, such as those causing Small-Delay Defects (SDDs), are difficult to detect by advanced test methodologies [1]. SDDs due to resistive opens and resistive shorts are an important group of defects in modern nanometer technologies. Experimental data have shown that the distribution of delay-related failures is skewed toward the smaller delays [2]. This means that the majority of devices that fail due to delay defects fail due to small delay defects [2]. Detection of these defects can be missed by typical and advanced test methodologies and can result in test escapes [3,4]. These defects can degrade with use leading to a reliability risk [1,5,6]. Furthermore, significant process variations in modern technologies pose major challenges to detect SDDs. Hence, there is strong interest for developing new test techniques targeting SDDs that lead to higher product quality.

Timing-aware pattern generation tools for testing SDDs have been proposed [7,8]. In this methodology, timing information is integrated into the ATPG. Kruseman et al. [9] propose grouping conventional delay-fault patterns into sets of almost equal-length paths to improve SDD detection. Tayade and Abraham [5] have found that the probability of detecting a delay defect on a net is higher using a path with lower delay variance. This property is used in a test pattern generation strategy. Yilmaz et al. [10] have proposed to use of *output deviation probability* as a criterion to select the optimal paths for SDD screening. Pei et al. [11] have proposed to use *faster-than-at-speed* clock frequencies to highlight the effects of SDDs. Favalli and Metra [12] propose the use of pulse propagation characteristics with on-line test structures to screen SDDs in non-critical paths. Yan and Singh [13] have proposed a test technique that can identify abnormal delays in the slack interval. They propose to compare the relative delay measures between neighboring dies of a wafer. In this technique, the variations on switching delays between neighboring dies is expected to be small. This property could be more difficult to accomplish for some advanced technologies. More recently Qian and Singh [14] have proposed a test strategy to distinguish resistive small delay defects from random parameter variations. They propose to observe the relative change to switching delay of the slow path with variation in the power supply voltage. They exploit the fact that the relative delay contribution of a performance outlier transistor increases with decreasing V_{DD}, while the relative delay contribution of a

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resistive delay defect decreases with increasing V_{DD} [14]. To observe the switching delays, the signal must be captured using a multiple clock scheme.

In this work, a novel methodology, based on analyzing the output delay correlation of two logic paths, able to detect SDDs in the slack-time interval and to distinguish SDDs from process variations is proposed. Our proposal has the benefit that is less impacted by die-to-die process variations and intra-die spatial correlation. Our methodology exploits the concept that for two correlated paths, a part of the delay variance in one path can be described by the delay variance in the second path. Delay output measurements for a pair of paths must agree with its *Inter-Path Correlation*. Otherwise, a defect is present in one of the paths. The output delay measurement is made by observing the output at multiple time delay intervals [13]. A statistical timing analysis framework is developed and implemented to compute timing information and inter-path covariance to estimate the inter-path correlation. This considers spatial and structural correlations, and random dopant fluctuations. Simulation results on ISCAS85 benchmark circuits indicate the feasibility of the proposed methodology.

This paper is organized as follows. Section 2 presents the proposed methodology to detect SDDs using inter-path correlation. Section 3 describes the inter-path delay correlation computation and define some metrics. Section 4 presents the simulation results of the application of the proposed methodology to ISCAS85 benchmark circuits. A comparison of our methodology with conventional delay testing is made. Section 5 discuss some test application issues. Finally, Section 6 gives the conclusions of this paper.

2. Delay testing of SDDs using inter-path correlation information

2.1. Detection of SDDs using inter-path delay correlation with single path prediction

A novel methodology to screen SDDs under process variations based on analyzing the inter-path delay correlation information between logic paths is proposed. Let us consider two logic paths of a circuit with output delays statistically modeled by normal distributions represented by $X \approx N(\mu_X, \sigma_X)$ and $Y \approx N(\mu_Y, \sigma_Y)$ having an inter-path delay correlation lower than 1. μ and σ are the mean and the standard deviation of the delay distributions of the paths. Fig. 1 shows graphically the delay values that X and Y can take to agree with a given correlation relationship between the delay distributions of the two logic paths. These delay values must fall in the region defined by the dotted lines. Even more, for a given sample delay value X_1 of a circuit, the obtained delay sample Y_1 of the same circuit (e.g. X_1 and Y_1 values of the fabricated die) is expected to fall in a detectable delay window. If the value of Y_1 locates out of the detectable delay window, then the paths does not agree with the correlation relationship between them, and hence a SDD is detected. The detectable delay window can be considered to be normally distributed with $Y_{1,FC}$ and $\sigma_{e_{X,Y}}$ as mean value and standard deviation, respectively. $\sigma_{e_{X,Y}}$ is known as the Standard Error of Estimation [15]. The amount of detectable delay in path Y, for sample X_1, depends on the location of sample Y_1 in the detectable delay window. The detectable delay is smaller as the value of sample Y_1 locates closer to the upper line $Y_{1,U}$ (See Fig. 1).

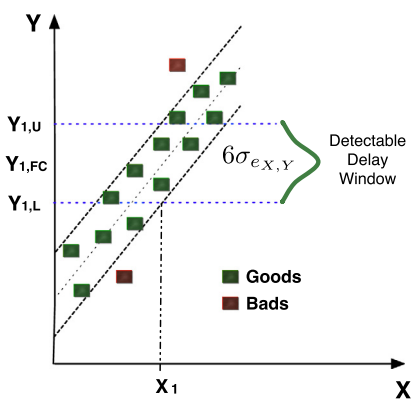

Fig. 1. Allowed delays (detectable delay window) for a measured delay value in path X.

The *Standard Error of Estimation* can be computed by the following expression [16],

$$\sigma_{e_{X,Y}} = \sqrt{\sigma_Y^2(1-\rho_{X,Y}^2)} \tag{1}$$

Note that the standard error of estimation depends on the variance of the variable to be estimated and the correlation between the delays of the two paths of interest. $6\sigma_{e_{X,Y}}$ defines the worst case delay detection (See Fig. 1) using inter-path correlation.

2.2. Detection of SDDs using inter-path delay correlation with multiple path prediction

In practice, logic paths have correlation degrees lower than 1 ($\rho < 1$). For instance, the delay of two logic paths having a correlation between them of $\rho = 0.8$ gives $\rho^2 = 0.64$. This means that 64% of the delay variance of a path can be associated with the delay variance in the other path, but there is still 36% that can not be described. Other predictive paths (multiple path correlation) can be used to relate part of the remaining 36% which allows to increase the inter-path correlation. In this approach, a set of predictive paths ($P_1 \cdots P_n$) are selected for having a larger portion of the variance of the path under test related to the variance of the predictive paths. This allows to reduce the standard error of estimation, and hence, to detect lower values of SDDs. The standard error of estimation using multiple path correlation can be computed as indicated in [17].

2.3. Impact of random independent variations

The impact of random independent variations on the detectability of small delays using the proposed methodology has been analyzed. The proposed methodology has been applied to a custom-designed paths using 180 nm TSMC standard library cells and Mentor Graphics tools. The circuit of Fig. 2 is considered as the path under test and circuit of Fig. 3 is considered the predictive path. The coordinates (x, y) of the gate's spatial location are given below each gate. The mean and the standard deviation of the path under test and the predictive one are given in Table 1.

Table 2 shows the impact of independent variations (e.g. RDF) on the detectability of small delays. This is shown for the original σ_{RDF}, $3\sigma_{RDF}$ and $6\sigma_{RDF}$. It can be observed that the standard deviation of the estimation error increases as the standard deviation of RDF increases. However, for σ_{RDF} and $3\sigma_{RDF}$ the standard deviations of the estimation error are significantly lower than the standard deviations of the path under test. Even, for $6\sigma_{RDF}$ there is an important difference. Our proposed methodology should be able to detect delay defects values smaller than using conventional delay testing. This is because, our approach makes a comparison of relative measurements, and the value of the detectable delay decreases for those dies fabricated closer to the upper line as shown in Fig. 1.