Microelectronics Reliability 54 (2014) 773–777

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Void control during plating process and thermal annealing of through-mask electroplated copper interconnects

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ARTICLE INFO

Article history:
Received 3 August 2013
Received in revised form 25 November 2013
Accepted 23 December 2013
Available online 22 January 2014

ABSTRACT

The quality of the sputtered copper film, which serves as the seed layer for sequent electroplating, becomes critical when the size of crack on the surface of the sputtered film is close to the feature size of the electroplated copper interconnect. The crack results in void formation in electroplated copper before thermal annealing and this phenomenon limits attainable highest anneal temperature. To solve this problem, the sputtered seed layer was slightly etched before electroplating process and a TaN passivation layer was deposited on the electroplated Cu interconnect before thermal annealing. Those processes not only suppressed void formation during the electroplating and annealing process at 300 °C, but also resulted in lower electrical resistance in the copper interconnects.

1. Introduction

Copper interconnects are widely used in ultra large scale integrated (ULSI) circuits to distribute clock and other signals, and to provide power/ground to the various circuits for its low resistivity. Low resistance will decrease interconnect resistive–capacitive (RC) delay and increase the circuit speed. Advances in circuit speed have been obtained by downward scaling of feature sizes of transistors in the circuits since smaller transistors inherently reduce RC delay. Currently, however, the speed limit of advanced ULSI circuits is determined by the RC delay in the metal interconnect lines [1]. Since the copper interconnects with larger grain size is beneficial to lower resistance and higher circuit speed, thermal annealing is preferred to initiate and promote the grain growth [2]. Thermal stresses induced in the annealing as well as potential impacts on the mechanical and electrical reliability of 3-dimensional integration have been investigated [3]. The typical annealing process for copper is performed in a furnace at 100 °C for 60 min to reduce the structure energy by reducing the grain boundaries within the copper interconnect. To achieve larger grains and lower resistance, higher annealing temperature is critical. The researchers have carried out an anneal process at 300 °C for 10 min and found void formation in the copper plated using damascene process. The voids increase the electrical resistance, and limit the attainable maximum anneal temperature [4]. They incorporated a TaN layer to prevent void formation in the copper during thermal annealing process [2].

As the void problem occurs in the damascene plating copper, it is possible there are voids in the through-mask plating copper when subjected to the thermal annealing at relatively high temperature. Through-mask plating is widely used in the semiconductor packaging industry, especially in wafer lever chip scale package (WLCSP). As shown in Fig. 1, the two plating processes are not exactly the same. For through-mask plating, the seed layer is sputtered on the wafer surface. Then photoresist is deposited and patterned. Electroplating occurs only in the lithographic areas that are not covered by the photoresist. After electroplating, the photoresist and the unneeded seed layer are removed. In Damascene processing, the seed layer is deposited on top of the patterned material, which is a part of the structure, and therefore, electroplating occurs all over the seed layer. Excess copper (called overburden) must be removed by the chemical–mechanical polishing (CMP) [5]. Some differences can be observed between the two plating processes. Firstly, overburden will appear in the damascene process and provide the path for mass transportation, which is driven by the stress gradient in the overburden [2]. In damascene process, the copper is buried in the dielectric material during the fabrication process and a rigid barrier layer will be deposited before the deposition of seed layer to improve the seed layer adhesion. This barrier will enclose the Cu interconnect. But in through-mask plating method adopted in WLCSP, barrier layer is only deposited at the bottom of Cu interconnects and the other surfaces are free constrained. The confinement will have effect on the void formation in Cu interconnect.

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http://dx.doi.org/10.1016/j.microrel.2013.12.019

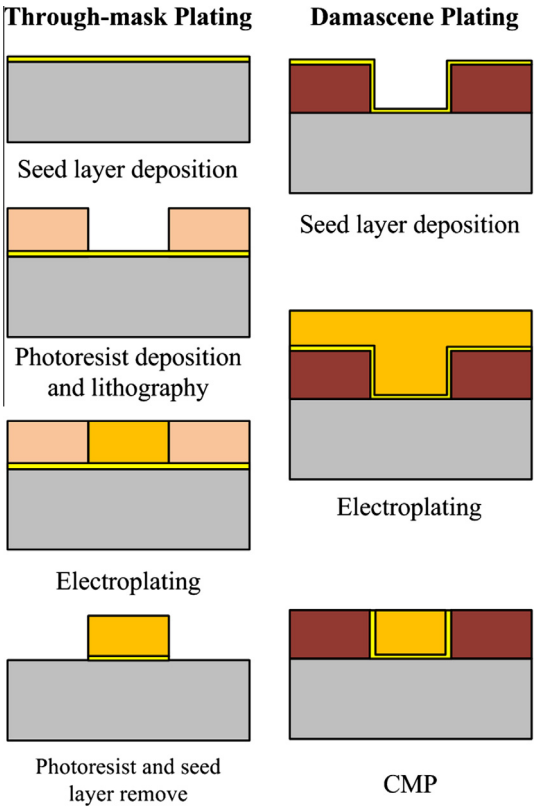

Fig. 1. Two plating methods.

Due to the above factors, whether the through-mask plating copper is able to withstand the thermal annealing process without void formation is unpredictable yet. For this, we fabricated the copper line samples using through-mask plating process and found that there were voids in the plated copper even before thermal annealing. These voids not only increase the electrical resistance as mentioned in C.C. Yang's work [2], but also have potential effects on the grain growth in the following thermal annealing process, for the imperfections make it difficult to reduce the grain boundaries generally.

In this paper, the process to eradicate the voids during plating process and sequent thermal annealing process in through-mask copper plating process was reported.

2. Sample preparation

2.1. Sample preparation process

The sample was fabricated using through-mask plating process. The control reference consists of 1 μm electroplated Cu/0.4 μm sputtered Cu/0.1 μm sputtered Ti/0.5 μm SiO_2/Si. The dimension of the electroplated copper line is 5 mm × 10 μm × 1 μm, with a pitch of 20 μm.

2.2. Thermal annealing process

Thermal annealing was carried out to investigate its effects on the electroplating copper. Thermal annealing process included no thermal annealing, 100 °C for 60 min, 200 °C for 10 min, and 300 °C for 10 min. The process was performed in a reflow oven (SRO-704) with a Nitrogen atmosphere. To evacuate the oxygen, the oven was vacuumed up by a molecular pump firstly and then the nitrogen gas was poured into.

2.3. Void observation

FIB (Quanta 3D FEG 200/600, FEI) was used to cut the copper samples to investigate the voids in the electroplated copper, as shown in Fig. 2.

2.4. Stress measurement

The stress relaxation behavior of two film stacks without patterns was examined by the substrate curvature method. The substrate curvature method has been described in detail in literature [6]. The temperature ramped up to 375 °C with a rate of 5.8 °C/min and kept constant at 375 °C for 30 min. Then it cooled to the relaxation test temperature of 175 °C with a rate of 7.3 °C/min. The temperature was constant within 0.2 °C during the isothermal stress relaxation.

2.5. Resistance measurement

Electrical resistance measurements were carried out on copper interconnects to further evaluate the impact of the voids. The measurements were performed using Agilent 4156C Precision Semiconductor Parameter Analyzer with the scan voltage ranging from −0.1 V to 0.1 V.

3. Results and discussion

3.1. Void distribution

The voids appeared on the interface between the sputtered copper and electroplated copper after electroplating and grew up after the sequent thermal annealing at 200 °C for 10 min, which are shown in Fig. 3(a) and (b) respectively.

3.2. Effects of cracks of the seed layer

After careful verification, cracks were observed on the surface of the seed layer after sputtering as shown in Fig. 4(a), which cannot be eliminated by adjusting the deposition parameter. It got worse after thermal annealing as shown in Fig. 4(b). The formation of cracks might be due to the tensile thermal stress induced when the sputtered layer cooled from deposition temperature, which is generated by the atomic bombardment in sputtering. Electroplating did not carry out in those cracks for theirs small feature size

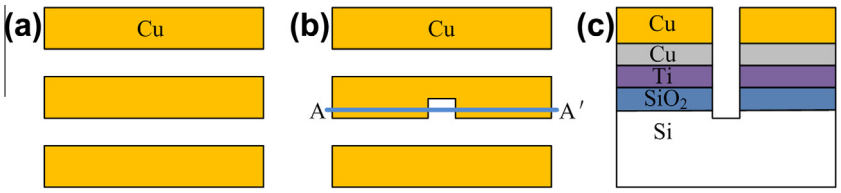

Fig. 2. Void observation using FIB. (a) The electroplating copper (top view), (b) copper after being cut by FIB (top view) and (c) details of AA′(side view, observation direction).