Physica B 512 (2017) 91–99

Contents lists available at ScienceDirect

Physica B

journal homepage: www.elsevier.com/locate/physb

A unique structure for the multiplexer in quantum-dot cellular automata to create a revolution in design of nanostructures

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ARTICLE INFO

Keywords:
Quantum-dot cellular automata
Nanotechnology
Multiplexer
Unique structure

ABSTRACT

Quantum-dot cellular automata (QCA) is the advent of technology and suitable replacement for semiconductor transistor technology. In this paper, a unique structure for the 2:1 multiplexer is presented in QCA. The structure of this component is simple, ultra-efficient and very useful to implement the various logical functions. The proposed structure does not follow any Boolean function. It takes advantage of the inherent characteristics of quantum technology to produce the desired output. Based on these principles, we design the new and efficient structures for the 4:1 multiplexer and 8:1 multiplexer in the QCA technology. These structures are designed with QCADesigner simulator and simulation results are examined. Investigation results indicate the amazing performance of proposed structure compared to existing structures in terms of area, complexity, power consumption and latency.

1. Introduction

Being small manufacturing technology in CMOS circuits allowed designers to consider CMOS as a business plan. In recent years, there are remarkable evidences such as leakage current and high power consumption [1] in CMOS circuits. Therefore it is important that the technology revolution happen in CMOS [1]. CMOS technology based on today's traditional transistors, Follow Moore's Law [2]. Increasing transistors inside the chip is unpleasant in CMOS technology, but there is a plan at the nanoscale that shows us the possibility of changing the Moore's Law, which is quantum-dot cellular automata (QCA) technology that violated Moore's Law by replacing the new technology with CMOS technology easily [3,4].

The QCA technology has the ability to build circuits with high speed and low latency than the CMOS technology [4–6]. Recent advances in QCA have enabled this technology to build diverse digital components such as XOR gate and multiplexer with the lowest occupation area [7,8]. The multiplexers have wide applications in digital circuit implementation such as ALU, RAM cells and etc [4,9,10,29–32].

The rest of this paper is organized as follows: first, we review the background about QCA in the next section and then we describe the proposed 2:1, 4:1 and 8:1 multiplexer architectures. In the next, we present the simulation results and evaluation discussion. The conclusion is appeared at the end.

2. Background

Quantum-dot cellular automata is a new technology that is suitable for the nanoscale circuits [11]. This technology is based on interaction of quantum cells in circuits. The quantum cells are in square forms and have four quantum dots. These quantum dots are located on the corners of a square and included two electrons [12]. Quantum-dot is an area to resident an electron mechanically as shown in Fig. 1(a) and electron tunnels among the points in quantum mechanical mode and remains there as shown in Fig. 1(b). This operation creates two different polarizations in the cell that are known as P=+1 (logic 1) and P=−1 (logic 0).

The QCA wire is formed by an array of QCA cells as shown in Fig. 2(a) and Inverter gate can be constructed by different configuration of QCA cells as shown in Fig. 2(b) and (c). The other main structure in QCA is three-input majority gate as shown in Fig. 2(d). The two-input “OR” and “AND” gates can be constructed by fixing one of the inputs of the three-input majority gate to polarization “+1” and “−1”, respectively.

In order to construct sequential QCA structures, needs to use clock scheme. A QCA cell has four clock zones and each clock zone has four phases; Switch, Hold, Release and Relax; as shown in Fig. 3. In first phase, cell is non-polarized and the potential barrier among quantum-dots is down. During this phase, barrier gone up and the cells begin to polarize according to its own input. In the second phase or the Hold phase, barrier is kept high. So output of sub-array can be used as an

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http://dx.doi.org/10.1016/j.physb.2017.02.028
Received 11 January 2017; Received in revised form 18 February 2017; Accepted 20 February 2017
Available online 21 February 2017

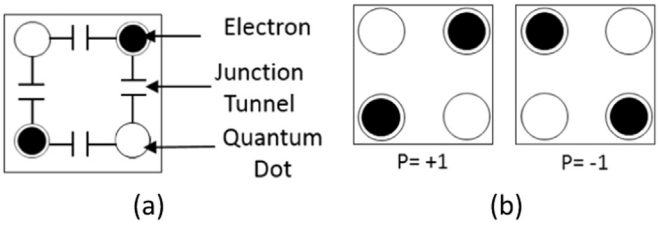

Fig. 1. (a) QCA Cell; (b) Quantum-dot cell with two different polarizations.

input in next class. In the third phase or Release phase, barrier is lowered and the cells will be allowed to start going in internal polarity state. Finally, cell barriers remain lowered and cells remain in a non-polarized state during the fourth phase [13].

3. Related works

In this section, we provide a brief description of the 2:1 multiplexer operation as well as we review some recent previous structures. Multiplexer is a hybrid circuit that receives information from 2^n input lines and transmits one of them to an output line in each moment based on select signals. A 2^n:1 multiplexer contains 2^n information input lines and n select input lines that determine which information input line is selected as the output.

The recent previous 2:1 multiplexer architectures are shown in Fig. 4. A 2:1 QCA multiplexer design proposed in [24] as Fig. 4(a). This design consists of 27 cells, 0.03 μm^2 area and 3 clock zones latency. The other structure for 2:1 multiplexer proposed in [18] as Fig. 4(b). This structure has 26 cells, 0.02 μm^2 area and 2 clock zones latency. The proposed structure in [4] for 2:1 QCA multiplexer is shown in Fig. 4(c). This design has 23 cells, 0.02 μm^2 area and 2 clock zones latency. Fig. 4(d) shows another design for 2:1 QCA multiplexer that proposed in [26] and has 15 cells, 0.01 μm^2 area and 2 clock zones latency.

The output of the 2:1 multiplexer proposed in [24] is given by $out=\overline{S}.A+S.B$, that A and B are the two data input lines and S is the select line. The implementation of this structure in the majority gate representation is shown in Eq. (1). That is, three majority gates and one inverter are necessary to implement a 2:1 multiplexer.

$$Out = Maj\,(Maj\,(B,\ \overline{S},\ 0),\ Maj\,(A,\ S,\ 0),\ 1) \quad (1)$$

The output of a 2:1 multiplexers proposed in [4,18,26] are given by $out=S.A+\overline{S}.B$, that A and B are the two data input lines and S is the select line. The implementations of these structures in the majority gate representation are shown in Eq. (2). That is, three majority gates and one inverter are necessary to implement a 2:1 multiplexer.

$$Out = Maj\,(Maj\,(\overline{S},\ A,\ 0),\ Maj\,(S,\ B,\ 0),\ 1) \quad (2)$$

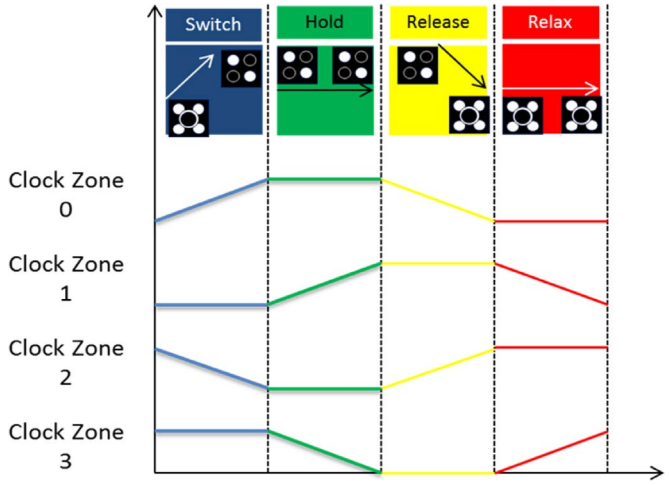

Fig. 3. QCA clocking scheme.

4. Proposed structures

In this section, first, a unique and ultra efficient structure is proposed for 2:1 multiplexer. Then, a new structure is designed for 4:1 multiplexer and 8:1 multiplexer using the proposed unique structure.

4.1. Proposed 2:1 QCA multiplexer structure

Truth table of the 2:1 multiplexer is illustrated in Table 1. As can be deduced from the table, when *S=0* the output is equal to "*I0*" and when *S=1* the output will be equal to "*I1*".

We use only a new gate called the MUX gate to design a 2:1 multiplexer. The schematic and QCA layout of this gate are shown in Fig. 5(a) and (b), respectively. The proposed structure has two inputs, one selector and one output. The inputs are *I0* and *I1* and output is *OUT*. The signal *S* is selector signal. Selector can connects *I0* to the *OUT* when *S=0* and input *I1* to *OUT* when *S=1*. The logic function of proposed MUX gate can be presented as Eq. (3).

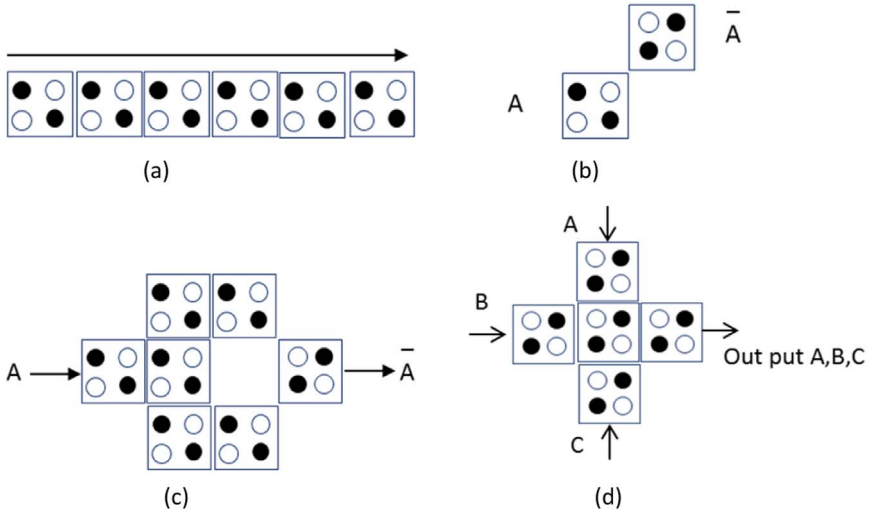

Fig. 2. Basic QCA logical devices, (a) wire; (b) and (c) inverter; (d) three-input majority gate.