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Thin hybrid pixel assembly fabrication development with backside compensation layer ☆

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ABSTRACT

The ATLAS and CMS experiments will both replace their entire tracking systems for operation at the HL-LHC in 2026. This will include a significantly larger pixel systems, for example, for ATLAS approximately 15 m^2. To keep the tracker material budget low it is crucial to minimize the mass of the pixel modules via thinning both the sensor and readout chip to about 150 μm each. The bump yield of thin module assemblies using solder based bump bonding can be problematic due to wafer bowing during solder reflow at high temperature. A new bump-bonding process using backside compensation on the readout chip to address the issue of low yield will be presented. The objective is to compensate dynamically the stress of the front side stack by adding a compensating layer to the backside of the wafer. A SiN and Al:Si stack has been chosen for the backside layer. The bow reducing effect of applying a backside compensation layer will be demonstrated using the FE-I4 wafer. The world's first results from assemblies produced from readout wafers thinned to 100 μm with a stress compensation layer are presented with bond yields close to 100% measured using the FE-I4 readout chip.

1. Introduction

The discovery in 2012 of the Higgs boson by the ATLAS [1] and CMS [2] collaborations was a great triumph for Particle Physics. Many particle physics questions, however, remain unanswered. The present ATLAS and CMS detectors will run until the end of 2022 and collect data from an expected 300 fb^{-1} of integrated luminosity. Many physics signatures require a significant increase in integrated luminosity to be measured, which will be provided by the high luminosity LHC, (HL-LHC [3]), with a planned start date of 2026. The HL-LHC has the goal of achieving an ultimate instantaneous levelled luminosity of 7.5×10^{34} cm^{-2} s^{-1}, resulting in a total integrated luminosity of 3000 fb^{-1} by 2035. The instantaneous luminosity corresponds to an approximate average of 200 additional pp collisions per beam-crossing, a factor of four higher than the LHC ultimate design.

The increased instantaneous luminosity leads to major challenges to the inner trackers of ATLAS and CMS, including increased detector occupancy, higher radiation damage and higher data transmission rates. As a consequence the inner trackers have to be re-designed to cope with these challenges while maintaining, or even improving, their tracking efficiency, fake rate and b-tagging capabilities. The ATLAS tracker, for example, will be an all silicon tracker with 5 pixel barrel layers and 4 strip barrel layers of back-to-back single sided silicon strip sensors. The pixel endcaps will consist of rings with a pseudo-rapidity coverage up to 4. The pixel system will comprise of up to 14,000 modules, the majority of which will be 4-chip devices with 134,400 pixels per readout chip (ROIC). To maintain the tracker's performance the material budget of every component must be minimized, while maintaining performance throughout the lifetime of the experiment. The large number of pixel modules will result in the modules themselves contributing a significant percentage of a radiation length. Thin pixel modules are therefore required throughout the entire pixel system. However, due to the large number of modules a thin module mass production technique is required, with a target thickness of 150 μm each for the ROIC and sensor being pursued for the ATLAS system.

For the CLIC [4] experiment the design goals are different from the general purpose LHC experiments driven by their precision physics program. A design goal of the vertex detector is a single point resolution of 3–5 μm. This is possible with a pixel detector system with a material budget of only 0.2% of a radiation length

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and pixel sizes of 20 μm × 20 μm. To achieve this with a hybrid pixel system a required ROIC thickness is only 50 μm, with an equal sensor thickness.

This paper describes the development of a wafer level approach to post-process the backside of the pixel ROIC wafer to allow thin hybrid pixel modules to be produced in a very similar fashion as thicker ones.

2. Manufacture of thin hybrid pixel modules

Hybrid pixel detectors are manufactured using a micrometre sized solder bump-bond (either tin-lead, silver-tin or indium) and flip-chip process. The ROIC and sensor wafers usually arrive from the vendors with an aluminium top metal layer. A solder wettable metal, known as the under-bump metal (UBM), is deposited upon the aluminium. A solder ball/pillar (or copper pillar with a solder cap) is deposited upon the UBM. The solder may be added to both the sensor and ROIC wafer, to reduce cost the solder is only deposited upon the larger ROIC wafer. The ROIC and sensor die are diced from the wafer, aligned and bonded on a flip-chip machine to produce a pixel assembly. To obtain the required electrical and mechanical quality the assembly is placed in a reflow oven and heater to the solder reflow temperature in a reducing atmosphere to remove any oxide layers. The reflow process has the additional advantage of producing self-alignment of the two die.

Issues with thin-chip processing: The ROIC used for the present ATLAS IBL [5] (the FE-I4 chip [6]) has eight metal layers on the front side above the CMOS circuit, each of which is separated by a silicon oxide or nitride layer. This is known as the back-end-of-line stack (BEOL). The first five are thin (0.3–0.6 μm) copper layers, and the sixth is a thin aluminium layer (0.5 μm). The final two layers are significantly thicker and used for power (3 μm copper) and shield (4 μm aluminium top layer). The total thickness of the BEOL stack is 16 μm. In addition to the BEOL stack 20 μm tall solder bumps are deposited on the ROIC. The BEOL and solder balls have a significantly different coefficient of thermal expansion (CTE) to that of the silicon wafer and are deposited at temperatures above room temperature. The thermal expansion mis-match between the BEOL and substrate causes a thermal stress in the plane of the ROIC (biaxial stress), resulting in a strain in the ROIC that bows the ROIC. The radius of curvature of the ROIC, r, is given for an isotropic film of thickness, t_f, and biaxial stress σ_f by Stoney's model [7] as

$$r = \frac{E_s \times t_s^2}{(1 - \nu_s) \times 6 \times \sigma_f \times t_f} \quad (1)$$

where E_s is Young's modulus, ν_s is the Poisson ratio and t_s is the thickness of the substrate. The thermally induced stress in the thin film is equal to the product of Young's modulus of the thin film, E_f, the difference in the CTE of the film and substrate (α_F and α_s) and the difference in the film deposition temperature and measurement temperature ($T_{dep} - T_{mea}$). The smaller the radius of curvature the larger the bow of the wafer. The FE-I4 ROIC BEOL is non-isotropic however the Stoney's equation is a good illustration of the effect to be managed.

The substrate of the 130 nm IBM process used for the FE-I4 ROIC is 750 μm thick which is sufficient to resist the stress from the BEOL at room temperature resulting in almost flat die. Reducing the substrate thickness however will reduce the radius of curvature rapidly.

Topography and Deformation Measurement (*T.D.M.*) *of thin ROIC under thermal load*. The bow of the FE-I4 die was characterised as a function of temperature using the Topography and Deformation Measurement, TDM-HR [8], equipment from Insidix[1] which has a full-field and fast acquisition mode to measure optically the deformation of the sample under a thermal load. The non-contact measurement technique is based on the projection Moire principle. Structured light is projected onto the sample and the reflected light is captured by a CCD camera. The reflected light pattern is characteristic of the sample's surface structure. The sample is heated with infrared lamps from both the top and bottom sides to guarantee a uniform device temperature. The out-of-plane resolution of the optics is ±3 μm and in-plane (x, y) detection ability is $\Delta L/L = 5 \times 10^{-5}$. The ROIC was measured from the backside of the die and all measurements are quoted relative to the backside.

The die were thermally cycled from ambient to the solder reflow temperature (260 °C) and back to ambient for three identical cycles. The backside of the die was imaged in the TDM to produce a surface displacement contour map, an example is shown in Fig. 1 for a 100 μm thick FE-I4 die with front side microbumps. The die deformation follows a smooth spherical shape and does not show structure due to the pixel columns. The bow, or warpage, of the die is defined as the difference between the maximum and minimum heights of the surface. In Fig. 2 three results are reported. The first two are for 100 μm thick FE-I4 die with and without front side microbumps, the third curve is discussed in Section 3.

At room temperature the chip is concave, with the microbumps on the inside of the concave surface, with a bow of +50 μm, in agreement with previous measurements obtained at a similar thickness [9]. During heating, two regions are observed. First a linear regime up to about 100 °C where the bow decreases and becomes negative to reach −120 μm, followed by a second asymptotical regime up to 260 °C where the bow continues to decrease smoothly to a minimum of −175 μm. During cool down two subsequent regimes were also observed, the first between 260 °C and 150 °C with a strong decrease of the bow followed by a second regime from 150 °C to ambient with a slower rate ending at +100 μm. During the second cycle the behaviour is similar, starting from the new origin and with a temperature shift of the linear portion of the heating curve, then during cool down the values are identical to the first cycle. The third cycle is identical to the second. The ROIC bow is driven by the ROIC's thick final metal layers. Upon heating, up to 100 °C, the first regime corresponds to the elastic deformation of the metal driven by the differential coefficient of thermal expansion between the aluminium/copper and the silicon, the plateau regime corresponds to the plastic deformation, or yielding, of the metal for high stress values. The same behaviour is observed upon cooling with an elastic regime followed by some yielding below 150 °C. Similar effects have been observed with Al:Si layers on silicon substrates [10]. The FE-I4 die without front side bumps has a similar bow at room temperature and a similar temperature dependence, but due to the lack of bumps the die bow is reduced by about 50 μm at 260 °C.

The overall change in bow of the die is 275 μm for a temperature change from room temperature to the solder reflow temperature. Such a large change in the shape of the ROIC results in the solder bumps of the pixel assembly failing during the solder reflow process. The soft solder bumps at the reflow temperature are insufficiently strong to resist the force of the bowing ROIC and the bumps pull apart. Assemblies fabricated with 200 μm thick FE-I4 die have shown bump yields as low as 30% due to this effect.

Existing technology used for the ATLAS IBL: There is an existing technology to fabricate thin ROIC hybrid pixel assemblies that has been developed at IZM [9] and successfully deployed for the ATLAS

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