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From vertex detectors to inner trackers with CMOS pixel sensors

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ABSTRACT

The use of CMOS Pixel Sensors (CPS) for high resolution and low material vertex detectors has been validated with the 2014 and 2015 physics runs of the STAR-PXL detector at RHIC/BNL. This opens the door to the use of CPS for inner tracking devices, with 10-100 times larger sensitive area, which require therefore a sensor design privileging power saving, response uniformity and robustness. The 350 nm CMOS technology used for the STAR-PXL sensors was considered as too poorly suited to upcoming applications like the upgraded ALICE Inner Tracking System (ITS), which requires sensors with one order of magnitude improvement on readout speed and improved radiation tolerance. This triggered the exploration of a deeper sub-micron CMOS technology, Tower-Jazz 180 nm, for the design of a CPS well adapted for the new ALICE-ITS running conditions. This paper reports the R & D results for the conception of a CPS well adapted for the ALICE-ITS.

1. Introduction

CPS integrate on the same silicon substrate the sensing elements and the front-end and readout circuitry (cf. Fig. 1). Impinging charged particles create electron-hole pairs in a moderately P-doped epitaxial layer located on top of a highly P-doped (P++) wafer substrate and below some highly doped P-well (P++) implants of the front-end circuitry. The generated electrons are collected on an N-well implanted on top of the epitaxial layer. In conventional CPS, the epitaxial layer is not fully depleted, and the electrons move mainly by thermal diffusion. However, they are deflected by built-in voltages of the P-epi/P++ interfaces which somewhat guide them toward the N-well/P-epi collection diode. Once collected, the charge is stored in the diode-parasitic capacitance, whose voltage drop is amplified by a low-noise in-pixel amplifier.

CPS feature the possibility of fine pixel pitch (down to 10 μm) providing a very good spatial resolution (typically a few μm). The very thin epitaxial layer (10 – 40 μm) allows to thin the sensor down to 50 μm, which turns into an exceptionally small material budget. Furthermore, the sensors can be operated at room temperature, avoiding to use complicated cooling systems which additionally contribute to the material budget.

A competitive tolerance to non-ionizing radiation (up to $10^{14} n_{eq}/cm^2$) was achieved when CMOS-processes with lightly-doped (so-called high-resistivity) epitaxial layer became available. This improved significantly the depletion depth up to several μm, dramatically accelerating the charge collection, an thus reducing the transit time around trapping-defects in the bulk generated by non-ionizing radiation.

The sensor's readout speed depends on the on-chip data processing circuitry. Initially, the signal from the in-pixel amplifier was multiplexed to a common analog readout bus and sent out for further processing, giving a few ms readout time ($t_{r.o.}$) for a sensor of larger sensitive area. A factor of 1000 reduction in $t_{r.o.}$ was obtained by reading in succession rows of the pixel matrix, allowing each pixel to send in parallel their signal to the column end, the so-called rolling shutter architecture. This data is then processed trough discriminators ending each column for digitization and then further processed by an on-chip data sparsification circuit. This allowed parallel column readout and reduced transmission band-width, shortening the $t_{r.o.}$ to about 100 μs.

All these developments allowed the conception of a CPS, called MIMOSA-28 [1] (cf. Table 1), suited to the STAR-PXL detector [2] operated at RHIC/BNL, the first vertex detector based on the CPS technology. The STAR-PXL has successfully participated in two data-taking campaigns and is currently in operation. It has proven to be reliable and to deliver the expected added value for the STAR physics program. The 400 sensors composing the PXL have allowed accumulating a sizable amount of experience with these devices.

The performance reached by the MIMOSA-28 sensor are not suited to match some of the more demanding requirements of the

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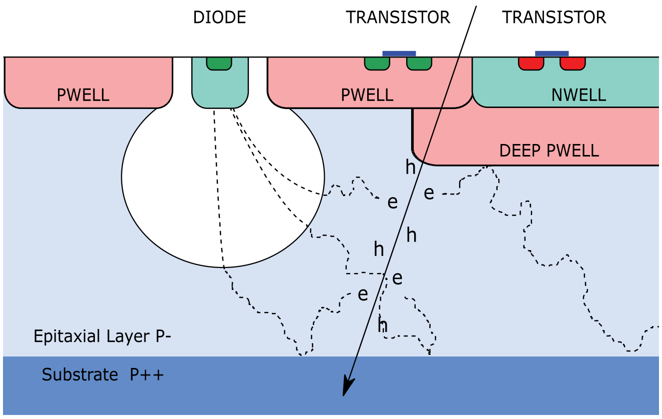

Fig. 1. Schematic cross-section of a CMOS pixel sensor.

Table 1
Properties (design goals for MISTRAL-O) of sensors discussed in this paper.

	MIMOSA-28	FSBB-M0	Mi-22THRb	MISTRAL-O
CMOS process	350 nm	180 nm	180 nm	180 nm
Pixels (col. × row)	960 × 928	416 × 416	64 × 64	832 × 208
Pixel pitch [μm^2]	20.7 × 20.7	22 × 33	39 × 50.8 or 36 × 62.5	36 × 65
Sensitive area [mm^2]	19.2 × 19.9	13.7 × 9.2	8.1 or 9.2	13.5 × 30.0
σ_{sp} [μm]	≳3.6	≳4.5	~10	~10
$t_{r.o.}$ [μs]	185.5	41.6	~5	20.8
TID [MRad]	>0.15	>1	>0.15	>0.15
NIEL [$10^{12} n_{eq}/cm^2$]	>3	>10	>1	>1
Power [mW/cm^2]	160	<160	N/A	≲80
Pads over pixels	No	No	Yes	Yes
On-chip sparsification	1D	2D	None	2D

Table 2
Sensors design goals of STAR-PXL (operational) and new ALICE-ITS inner (ITS-in) and outer (ITS-out) layers. σ_{sp} refers to the spatial resolution, and TID and NIEL to the ionizing and non-ionizing doses, respectively.

	STAR-PXL	ITS (in)	ITS (out)
σ_{sp} [μm]	<4	<5	<10
$t_{r.o.}$ [μs]	185.5	30	30
TID [MRad]	0.15	2.70	0.10
NIEL [$10^{12} n_{eq}/cm^2$]	3	17	1
$T_{operation}$ [°C]	35	30	30
Power [mW/cm^2]	160	<300	<100
Surface to cover [m^2]	0.15	0.17	>10

new ALICE-ITS [3] (cf. Table 2), mainly in terms of $t_{r.o.}$ and power consumption (outer layers), and to a lesser extent in terms of radiation tolerance[2] (inner layers). This triggered the exploration of a new 180 nm CMOS process with several advantages to overcome the limitations of the AMS 350 nm CMOS process used for MIMOSA-28. This document describes the features of the new CMOS process and its advantages as compared to elder ones. Furthermore, current status of the R& D for the conception of a sensor adapted for the ALICE-ITS outer layers is also presented.

[2] The ALICE-ITS doses in Table 2 are the ones reported in the TDR, but more detailed studies have shown that significantly lower doses need to be tolerated.

2. ALICE-ITS upgrade: R& D of sensors for outer layers

To overcome the limitations of the MIMOSA-28 sensor for the ALICE-ITS application, it was decided to migrate to the novel Tower-Jazz 180 nm CMOS process. One of its aspects is the smaller feature size, improving the $t_{r.o.}$ (higher integration density) and tolerance to ionizing radiation. Furthermore, the process grants thicker epitaxial layers with higher resistivity, improving the signal-to-noise ratio and tolerance to non-ionizing radiation. Finally, the new technology concedes for deep P-well implants which shield the N-well hosting PMOS transistors, preventing parasitic charge collection. This allows both PMOS and NMOS transistors to be used inside pixels, permitting to implement an in-pixel discriminator.

All these features widen the choice of the readout architecture strategy. An asynchronous readout similar to the one used for the hybrid pixel sensors [4] is pursued via the ALPIDE design [5], which is the most promising approach to equip the ALICE-ITS inner layers. This approach comes with certain risks of missing the project's tight schedule, as it requires building and testing a complex pixel matrix with several new features to be validated. In order to be on schedule it was decided to also follow a more conservative approach, the MISTRAL-O chip, using the validated rolling shutter readout of the MIMOSA-28 sensor. MISTRAL-O was intended to instrument the ALICE-ITS outer layers, which feature two orders of magnitude higher surface to cover, thus requiring special attention on power consumption, response uniformity and robustness.

MISTRAL-O needs to be about 10 times faster than MIMOSA-28 together with twice less power consumption (cf. Table 2). It has as well to be pin-to-pin compatible with the ALPIDE design, which includes pads over the pixel matrix suited to laser soldering. Furthermore, the sensor's slow control and digital logic need to be adapted to ALPIDE's standards.

2.1. Rolling shutter readout in the novel CMOS-process

As a first step for validating the new 180 nm CMOS-process, a full scale prototype called FSBB-M0 was built early in 2015 (cf. Table 1). The sensor includes a very similar analog front-end and digital readout chain as the MIMOSA-28 sensor with a $t_{r.o.}$ reduced by a factor of ~4. This was achieved by reducing the number of pixels in a column to be readout (928 → 416) and increasing the size of the pixel along the column (20.7 → 33 μm). Furthermore, the rolling shutter readout mode addresses simultaneously all pixels belonging to a pair of neighboring rows. Therefore, each discriminator addresses 208 pixels instead of 928, with a proportionnally reduced $t_{r.o.}$. The sensing nodes are staggered in order to maximize the uniformity of the sensing node density and to alleviate the spatial resolution asymmetry consecutive to the pixel's rectangular shape. Moreover, the sparsification circuit allows to find clusters of pixels in 2-dimensional windows instead of the 1-dimensional ones of MIMOSA-28, which had to be merged off-line.

Several FSBB-M0 sensors were first studied in the laboratory, where their temporal and fixed pattern noise performance were assessed over a wide range of positive temperatures. These measurements were performed before and after irradiation with an X-Ray source (up to 1.6 MRad) and with 1 MeV neutrons (up to $10^{13} n_{eq}/cm^2$), up to doses relevant for the ALICE-ITS inner layers (cf. Table 2). The sensors were next tested with particle beams at the CERN-SPS with negatively charged pions of ~120GeV/c, and at DESY with electrons of 3 – 6 GeV/c. Each set-up was made of six FSBB-M0 sensors operated simultaneously on beam. The performance of each sensor was assessed by considering it as a Device Under Test (DUT) and the rest as reference planes for track

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