Nuclear Instruments and Methods in Physics Research A ∎ (∎∎∎∎) ∎∎∎–∎∎∎

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

First prototypes of two-tier avalanche pixel sensors for particle detection

L. Pancheri [a,b,*], P. Brogi [c,d], G. Collazuol [e,f], G.-F. Dalla Betta [a,b], A. Ficorella [a,b], P.S. Marrocchesi [c,d], F. Morsani [d], L. Ratti [g,h], A. Savoy-Navarro [d,i]

[a] Università di Trento, Dipartimento di Ingegneria Industriale, I-38123 Trento, Italy
[b] TIFPA INFN, I-38123 Trento, Italy
[c] Università di Siena, DSFTA, I-53100 Siena, Italy
[d] INFN, Sezione di Pisa, I-56127 Pisa, Italy
[e] Università di Padova, Dipartimento di Fisica e Astronomia, I-35131 Padova, Italy
[f] INFN, Sezione di Padova, I-35131 Padova, Italy
[g] Università di Pavia, Dipartimento di Ingegneria Industriale e dell'Informazione, I-27100 Pavia, Italy
[h] INFN Sezione di Pavia, I-27100 Pavia, Italy
[i] University Paris-Diderot/CNRS-IN2P3, 75205 Paris Cedex 13, France

ARTICLE INFO

Article history:
Received 25 March 2016
Received in revised form
29 May 2016
Accepted 15 June 2016

Keywords:
Particle detector
Geiger-mode avalanche diode
CMOS
Pixelated sensor

ABSTRACT

In this paper, we present the implementation and preliminary evaluation of a new type of silicon sensor for charged particle detection operated in Geiger-mode. The proposed device, formed by two vertically-aligned pixel arrays, exploits the coincidence between two simultaneous avalanche events to discriminate between particle-triggered detections and dark counts. A proof-of-concept two-layer sensor with per-pixel coincidence circuits was designed and fabricated in a 150 nm CMOS process and vertically integrated through bump bonding. The sensor includes a 48 × 16 pixel array with 50 μm × 75 μm pixels. This work describes the sensor architecture and reports a selection of results from the characterization of the avalanche detectors in the two layers. Detectors with an active area of 43 × 45 μm^2 have a median dark count rate of 3 kHz at 3.3 V excess bias and a breakdown voltage non-uniformity lower than 20 mV.

1. Introduction

Several charged particle tracking applications call for the development of improved pixel detectors with low material budget and high spatial and temporal resolution, in addition to low power consumption and radiation hardness [1]. In order to meet these specifications, aggressive detector thinning has to be performed, but this operation strongly reduces the available signal, imposing severe constraints on the noise and uniformity of readout electronics.

To cope with this challenge, on the one hand the research community is striving to optimize silicon detectors and readout electronics, working both on the monolithic and hybrid approaches. From this point of view, progress in CMOS process technologies is beneficial, as device shrinking is continuously progressing and new features, such as 3D integration, are becoming more reliable. On the other hand, new detectors and new materials are being actively investigated with the goal of finding alternative and better performing solutions.

The introduction of avalanche gain is seen as an appealing perspective to recover the signal lost by device thinning and improving the timing resolution [2]. Low Gain Avalanche Detectors (LGAD), operating in sub-Geiger regime, could in principle reach a timing resolution in the order of tens of picoseconds.

Geiger-mode avalanche diodes have also been recently proposed as particle detectors [3,4]. These devices are currently well established for photon detection applications, and constitute the basic cells of Silicon Photomultipliers (SiPMs). However, their efficient use as particle detectors calls for a dramatic reduction of the dark count rate (DCR), which for SiPMs is typically of the order of 100 kHz/mm^2. To achieve this goal, the coincidence between two vertically-aligned avalanche detectors can be exploited, as illustrated in Fig. 1 [3]. Thanks to cell-to-cell coincidence, the dark count rate DCR_C of a two-layer pixel will be reduced to

$$DCR_C = DCR_1 \cdot DCR_2 \cdot 2\Delta T \quad (1)$$

where DCR_1 and DCR_2 are the dark count rates of the two cells, respectively, while ΔT is the coincidence time resolution.

This approach offers several advantages in applications requiring low material budget and fine detector segmentation as, for instance, for tracking and vertex reconstruction in particle physics

* Corresponding author at: Università di Trento, Dipartimento di Ingegneria Industriale, I-38123 Trento, Italy.

http://dx.doi.org/10.1016/j.nima.2016.06.094
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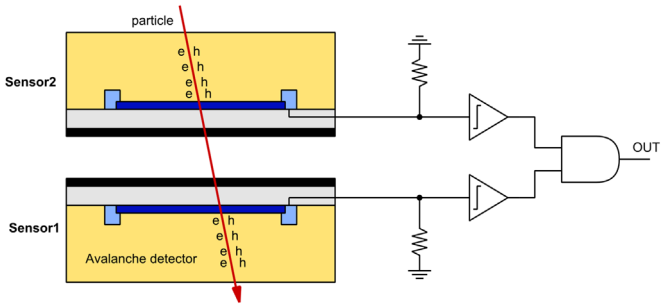

Fig. 1. Schematic illustration of coincidence detection principle.

experiments and charged particle imaging in medicine and biology. In addition, a timing resolution in the order of tens of picoseconds can potentially be achieved thanks to the fast onset of avalanche multiplication in Geiger-mode regime [5].

This detection mode was first studied exposing SiPM detectors to high energy particles of charge $Z=1$ and to ion beams with $Z>1$ [3,6]. The measurements have shown promising results, demonstrating a detection efficiency significantly larger than the geometrical fill factor of SiPMs.

To fully exploit the potential of this idea, however, it is necessary to monolithically integrate the readout electronics with avalanche detectors. Starting from the early 2000s, the co-integration of Geiger-mode avalanche diodes with readout electronics has been demonstrated in several CMOS technology nodes [7]. This has led to the realization of pixelated sensors for optical detection, a.k.a. Single-Photon Avalanche Diode (SPAD) arrays, for time-resolved sensing applicatons such as Time-of-Flight ranging and Fluorescence Lifetime Imaging [8].

The pixel particle sensor presented in this paper is based on the experience gained by the authors in the design of CMOS SPAD arrays. In our design, two layers of avalanche pixels are vertically integrated, with the coincidence detection performed at the pixel level.

The paper is organized as follows. Section 2 introduces the pixel concept and sensor design, while Section 3 presents a characterization of the avalanche detectors included in the two-layered structure. The main results are summarized in Section 4.

2. Chip design

A two-tier sensor assembly was designed and fabricated in a commercial 150 nm CMOS process. Two different types of Geiger-mode avalanche detectors were used in this design; their cross section is shown in Fig. 2. Type-1 detector has a shallow p+/nwell junction, while type-2 is based on a deeper pwell/deep nwell junction. Both devices are described in detail elsewhere [9,10].

In both cases, the active volume is less than 2 μm thick, and both detectors are isolated from the substrate thanks to a deep-nwell. On one hand, this can be an advantage if the sensors need to be thinned, since in principle it is possible to thin the dies down to a few micron without compromising its functionality. On the other hand, the fluctuations of the generated charge in such a small

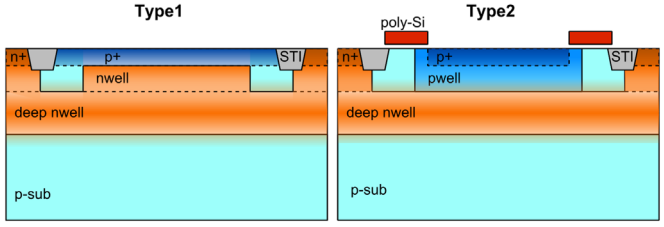

Fig. 2. Cross section of the two detector types.

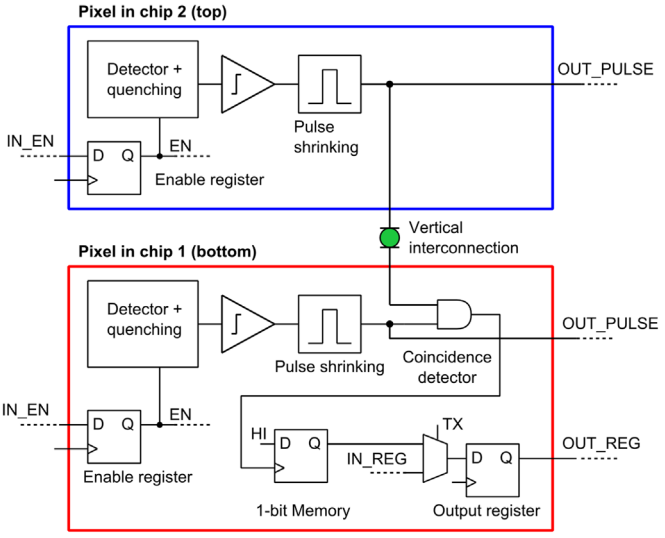

Fig. 3. Schematic diagram of two-layer pixel.

volume would be very large, and could lead to a loss of efficiency. An extensive experimental campaign will thus be necessary to accurately estimate the efficiency obtainable with this approach.

A simplified schematic diagram of the pixels, showing both layers, is sketched in Fig. 3. In the pixels, the detectors are passively quenched and their output signals are digitized by means of a low-threshold comparator. The resulting pulses are shortened by a programmable-length monostable circuit, providing a minimum pulse width of 750 ps. The pixels can be independently enabled or disabled with an arbitrary pattern, defined by a configuration register. The output of the monostable in the top half-pixel feeds a coincidence detector located in the bottom layer, and the coincidence output is stored in a 1-bit memory. Data from all the pixels can be transferred in parallel to an output register for readout and sent off-chip through 8 output pads. In this way, signal detection and data readout can be done simultaneously, thereby avoiding any dead time in the data acquisition process.

The monostable output signals are also sent to a row-wise OR gate, combining the outputs of all the active pixels in a row to a single signal stream. This feature was included to improve the testability of the chip and allows a wide range of tests if combined with proper setting of the configuration register, for example to map the dark count rate (DCR) between different pixels.

In addition, a row-wise coincidence detection circuit has also been included. The output of two given rows can be connected to the row coincidence detector, as shown in Fig. 4, allowing for the study of the coincidence among any arbitrary configuration of pixels between two rows. This feature can be used to measure the cross-talk between different pixels or groups of pixels in different rows.

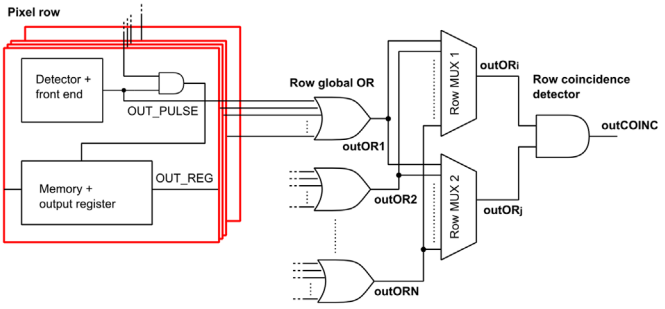

Fig. 4. Schematic diagram illustrating row-wise coincidence detection circuit.

Please cite this article as: L. Pancheri, et al., Nuclear Instruments & Methods in Physics Research A (2016), http://dx.doi.org/10.1016/j.nima.2016.06.094