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Thin n-in-p planar pixel modules for the ATLAS upgrade at HL-LHC

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ABSTRACT

The ATLAS experiment will undergo a major upgrade of the tracker system in view of the high luminosity phase of the LHC (HL-LHC) foreseen to start around 2025. Thin planar pixel modules are promising candidates to instrument the new pixel system, thanks to the reduced contribution to the material budget and their high charge collection efficiency after irradiation. New designs of the pixel cells, with an optimized biasing structure, have been implemented in n-in-p planar pixel productions with sensor thicknesses of 270 μ m. Using beam tests, the gain in hit efficiency is investigated as a function of the received irradiation fluence. The outlook for future thin planar pixel sensor productions will be discussed, with a focus on thin sensors with a thickness of 100 and 150 μ m and a novel design with the optimized biasing structure and small pixel cells (50×50 and $25 \times 100 \ \mu$ m²). These dimensions are foreseen for the new ATLAS read-out chip in 65 nm CMOS technology and the fine segmentation will represent a challenge for the tracking in the forward region of the pixel system at HL-LHC. To predict the performance of $50 \times 50 \ \mu$ m² pixels at high η , FE-I4 compatible planar pixel sensors have been studied before and after irradiation in beam tests at high incidence angle with respect to the short pixel direction. Results on cluster shapes, charge collection- and hit efficiency will be shown.

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1. Introduction

One of the main challenges for the innermost tracking detectors after the upgrade to the HL-LHC with an instantaneous luminosity of up to 5×10^{-34} cm⁻² s⁻¹ will be the exposure to high radiation. The ATLAS pixel system will be prospectively exposed to particle fluences up to 2×10^{16} n_{eq}/cm² (1 MeV neutron equivalent) [2,1]. To maximize the hit efficiency and reduce the leakage current and power dissipation after irradiation, thin sensors are being developed. Sensors with a thickness of 100 and 150 µm were found to reach the same hit efficiency as thicker sensors already at a bias voltage of 300 V shown in Fig. 1.

A highest hit efficiency of around 97% was obtained for perpendicular incident tracks at a fluence of $5 \times 10^{15} n_{eq}/cm^2$, the expected fluence for the second layer at HL-LHC [3]. The main inefficiencies are caused by the bias dot and the bias rail, as described in [4] for fluences up to $3 \times 10^{15} n_{eq}/cm^2$. In this paper, different designs of n-in-p planar hybrid pixel modules are investigated at the expected fluence of the second layer. Alternative biasing structures were implemented in a CiS sensor production with 270 µm thickness and compared to the standard design. To cope with the highest occupancy at HL-LHC, smaller pixel dimensions with respect to the ones presently implemented in the

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http://dx.doi.org/10.1016/j.nima.2016.05.113 0168-9002/© 2016 Published by Elsevier B.V. FE-I3 chip ($50 \times 400 \ \mu\text{m}^2$) and the FE-I4 chip ($50 \times 250 \ \mu\text{m}^2$), developed for the ATLAS Insertable B-Layer (IBL), are mandatory [5]. The new read-out chip for the ATLAS pixel systems at HL-LHC is being developed by the CERN RD53 Collaboration with a pixel cell of $50 \times 50 \ \mu\text{m}^2$ in the 65 nm CMOS technology and is expected to be ready at the beginning of 2017 [6,7]. Sensors compatible with this chip have been implemented in a recent MPG-HLL pixel production with a thickness of 100 and 150 μ m. First results on the electrical characterization of these devices will be shown.

2. Optimization of the pixel cell design

2.1. Test beam analysis of different pixel cell designs

In the present design of the ATLAS pixel sensors it is possible to bias the pixel via the punch-through mechanism with an n⁺ implant dot implemented in the pixel cell, connected to the bias ring through an aluminum rail. It has been observed that these structures introduce a loss of efficiency after irradiation [4,3]. To reduce this effect, an optimization has been carried out, comparing the performance of the different designs shown in Fig. 2. These were implemented in two FE-14 compatible sensors in a CiS n-in-p production on 6 in wafers with a thickness of 270 µm. The sensors were irradiated to a fluence of $5 \times 10^{15} n_{eq}/cm^2$ and then studied with a beam test at CERN SPS. The hit efficiency was determined

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Fig. 1. Comparison of hit efficiencies of FE-I4 modules with sensor thicknesses between 100 and 270 μm at an irradiation fluence of around $5\times 10^{15}\,n_{eq}/cm^2$.

performing track reconstruction with EUTelescope software [9]. The systematic uncertainty associated to the efficiency measurements is 0.3%, as estimated in [10]. Also at this higher fluence the relative performance remained similar to the one observed at $3 \times 10^{15} n_{eq}/cm^2$: the bias rail superimposed to the pixel implant as in Fig. 2b yields a higher hit efficiency with respect to the standard geometry. A still better hit efficiency was found for the common punch-through dot, placed externally to the pixel implant and serving four neighboring pixels, Fig. 2c. This geometry was implemented in a $25 \times 500 \ \mu\text{m}^2$ pixel cell, still compatible with the FE-I4 chip.

At a bias voltage of 500 V a hit efficiency of 93.9% was obtained for the standard design where the new arrangement of the bias rail in the modified design in Fig. 2b improved the hit efficiency to 94.6%. The common punch-through yields even 96.0%, while it increases to 98.0% at 800 V. These values are about 3% lower than what was obtained at a fluence of $3 \times 10^{15} n_{eq}/cm^2$. The smaller pixel dimensions of the future pixel read-out chips are indicated in the pixel cells in Fig. 2 using a 50×50 (a and b) and $25 \times 100 \ \mu m^2$ (c) pixel cell. A smaller pixel with the current designs would show even lower efficiencies. Therefore, further optimization of the biasing structures is mandatory. It is planned to repeat the hit efficiency measurements with sensors in a fluence range up to $10^{16} n_{eq}/cm^2$ to confirm the better performance observed within the new biasing design.

2.2. Estimation of hit efficiency for a $25 \times 100 \ \mu m^2$ pixel cell

Since modules with small pixel cells are not available yet, the hit efficiency for a 25 × 100 μ m² pixel cell at an irradiation fluence of 3 × 10¹⁵ n_{eq}/cm² was estimated based on the existing prototype of the 25 × 500 μ m² pixel cell with the new common punch-through design and is illustrated in Fig. 3. Since inefficiencies appear at the edges of the pixel caused by charge sharing as well as by the punch-through structure, the hit efficiencies in the first 40 μ m and in the last 60 μ m were combined to estimate the efficiency for an effective pixel cell of 25 × 100 μ m². A value of 95.5% was obtained and is indeed lower compared to the 25 × 500 μ m² pixel cell, but only a bit lower compared to the hit efficiency of 96.5% obtained with the standard implementation of the punch-through in a 50 × 250 μ m² pixel cell.

3. Performance at high incident angle

Since smaller pixel cells are challenging for the tracking in high pseudo-rapidity regions (high η), the hit efficiency for a cell of $50 \times 50 \,\mu\text{m}^2$ at $\eta = 2.5$ was determined. FE-I4 modules were placed in the beam at DESY and CERN SPS in such a way that the particles were crossing the pixel along the short side (50 μ m) at an angle of θ = 80°. Such measurements were previously performed at CERN with a 100 µm thick not irradiated module from the VTT production and at DESY with a 200 µm thick irradiated module from a CiS production. The cluster size along η strongly depends on the sensor thickness: thinner sensors produce smaller clusters and result in a lower pixel occupancy, as shown in Fig. 4. There was no possibility to reconstruct tracks for these data sets, implying that the analysis needs to be performed using the hit information of the long clusters compatible with the hypothesis a single particle passing through the sensor. Given the particle path of approximately 50 µm in each pixel cell, a collected charge of 3100 e was



Fig. 2. Hit efficiency for (a) the standard punch-through design and (b) the modified individual biasing structure where the bias rail is running over the bias dot after an irradiation fluence of $5 \times 10^{15} n_{eq}$ /cm². In addition the hit efficiency map of a pixel cell with the common punch-through design with modified dimensions to $25 \times 500 \ \mu\text{m}^2$ is illustrated in (c). Cut-offs of a $50 \times 50 \ \mu\text{m}^2$ pixel cell inside the $50 \times 250 \ \mu\text{m}^2$ pixel cell (a and b) and a $25 \times 100 \ \mu\text{m}^2$ pixel cell inside the $25 \times 500 \ \mu\text{m}^2$ pixel cell (c) are outlined. The modules were operated at $500 \ \text{V}$.

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