Nuclear Instruments and Methods in Physics Research A ∎ (∎∎∎∎) ∎∎∎–∎∎∎

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

The MuPix system-on-chip for the Mu3e experiment

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ARTICLE INFO

Article history:
Received 25 March 2016
Received in revised form
24 May 2016
Accepted 15 June 2016

Keywords:
Silicon sensors
Pixel detectors
Monolithic
CMOS
HV-MAPS
Mu3e

ABSTRACT

Mu3e is a novel experiment searching for charged lepton flavor violation in the rare decay $\mu^+ \to e^+e^-e^+$. Decay vertex position, decay time and particle momenta have to be precisely measured in order to reject both accidental and physics background. A silicon pixel tracker based on 50 μm thin high voltage monolithic active pixel sensors (HV-MAPS) in a 1 T solenoidal magnetic field provides precise vertex and momentum information. The MuPix chip combines pixel sensor cells with integrated analog electronics and a periphery with a complete digital readout. The MuPix7 is the first HV-MAPS prototype implementing all functionalities of the final sensor including a readout state machine and high speed serialization with 1.25 Gbit/s data output, allowing for a streaming readout in parallel to the data taking. The observed efficiency of the MuPix7 chip including the full readout system is ⩾99% in a high rate test beam.

1. The Mu3e experiment

The Mu3e experiment [1] will be carried out at the Paul Scherrer Institute (PSI) in Switzerland aiming to find or exclude the decay $\mu^+ \to e^+e^-e^+$ at a sensitivity level in a branching ratio of 10^{-16}, improving the current limit of 10^{-12} established by SINDRUM in 1988 [2] by four orders of magnitude. This requires operating the Mu3e experiment at very high muon stopping rates of $O(10^9$ Hz) for several years while keeping the background below the 10^{-16} level. In particular, background from radiative muon decays with internal conversion $\mu^+ \to e^+e^-e^+\nu\bar{\nu}$ needs to be suppressed by an excellent momentum resolution well below 0.5 MeV/c. Accidental background can be suppressed by a combination of precise time resolution of O(100 ps), vertex resolution of O (200 μm) and a very good momentum resolution. Since electrons and positrons from the muon decay at rest have a maximum momentum of 53 MeV/c, the momentum and vertex resolutions are limited by multiple Coulomb scattering. This requires the reduction of the detector material to 0.1 % of a radiation length X_0 per detector layer.

The Mu3e detector is composed of an extremely lightweight silicon pixel detector [3] surrounding a double cone target in a magnetic field of 1 T in combination with a scintillating fiber and a scintillating tile detector [4,5] for precise timing, see Fig. 1. The silicon pixel detector is based on high voltage monolithic active pixel sensors (HV-MAPS) thinned to 50 μm, readout via aluminium flex prints and mounted on Kapton® frames.

2. High voltage monolithic active pixel sensors

High voltage monolithic active pixel sensors [6,7] are pixelated detectors based on the commercially available HV-CMOS technology. Reverse biasing the deep N-well in the P-substrate with −60 V to −85 V leads to a depletion zone in the order of 15 μm thickness as reported in [7]. Ionizing radiation creates electron-hole pairs in the depletion zone. The electrons are collected via drift within 1 ns, see Fig. 2. Because of the very thin active detection layer, thinning to 50 μm is possible. In addition, CMOS analog and digital electronics can be implemented in the N-well so no extra readout chip is required.

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http://dx.doi.org/10.1016/j.nima.2016.06.095
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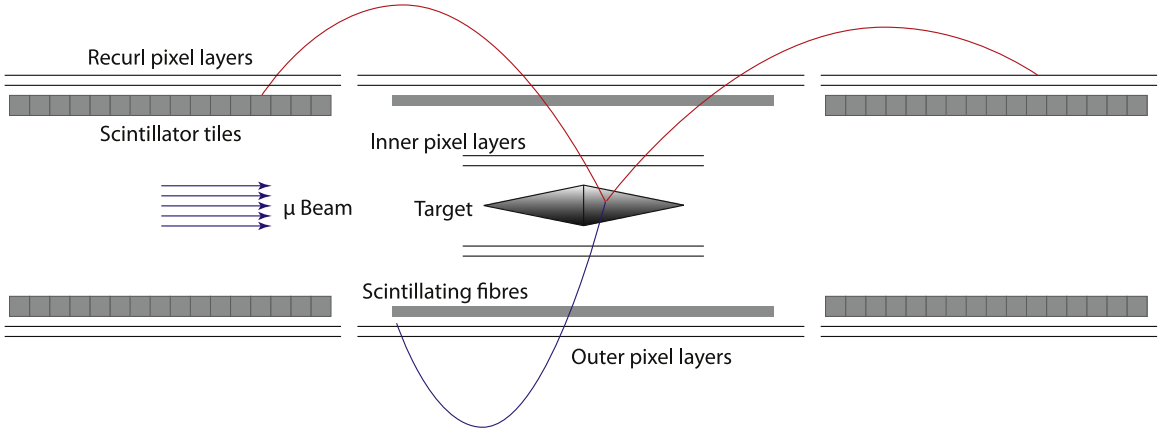

Fig. 1. Mu3e detector with signal event.

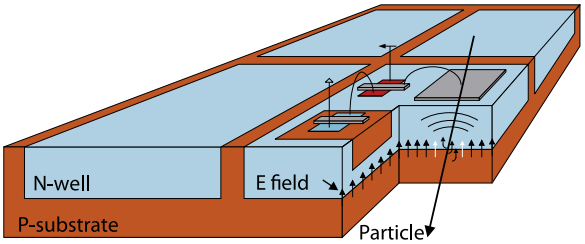

Fig. 2. HV-CMOS pixel detector scheme [6].

3. The MuPix system on chip

For the MuPix chip to be used in the Mu3e experiment, a pixel size of 80 × 80 μ m^2, an overall dimension of 2 × 2 cm^2 and a thickness of only 50 μ m is required.

Several smaller prototypes implemented in the AMS 180 nm HV-CMOS process have been extensively characterized [8-11]. A line driver in the pixel cell sends the analog pulse over a point-to-point connection to a corresponding digital pixel in the periphery. The signal is discriminated, a hit flag is registered and an eight-bit time-stamp is latched. Additionally, each digital pixel has a four-bit tune digital to analog converter (DAC) which allows to adjust the baseline for a common threshold in order to correct for pixel to pixel variations, see Fig. 3. The analog part with the preamplifier is implemented in the deep N-well above the sensitive pixel area, while the digital part is located in a small inactive region next to the pixel matrix in order to avoid digital crosstalk, see Fig. 4.

The MuPix7 prototype is the first in its series which integrates the complete readout circuitry, including a readout state machine, fast clock circuitry and fast serial output. At the beginning of each readout cycle, the hit flags of all pixels are copied to a second register. These registers drive a priority logic selecting the first hit in each column, which is then copied to a buffer in the column periphery. At the same time, the pixel hit flag is cleared and set ready to detect the next hit. A second priority logic identifies the first column with a hit, which is then sent to the fast output link. This is repeated until all column buffers are empty and the next hit in each column can be copied to the periphery. If all hits are read or an adjustable number of hits is surpassed, the cycle starts from the beginning. This readout is controlled by an on chip state machine running at 62.5 MHz and runs in parallel to the data taking. The only dead time incurred is in the hit pixels waiting for the copying to the column periphery. At low occupancy, this is comparable to the shaping time of around 1 μs. The output data consists of the row, column address and Gray-encoded time-stamp of hits interspersed with control words and synchronization counters. The data is 8b/10b encoded, serialized and sent off-chip via a 1.25 Gbit/s low voltage differential signaling (LVDS) link. The clocks required for the time-stamp generation, the readout state

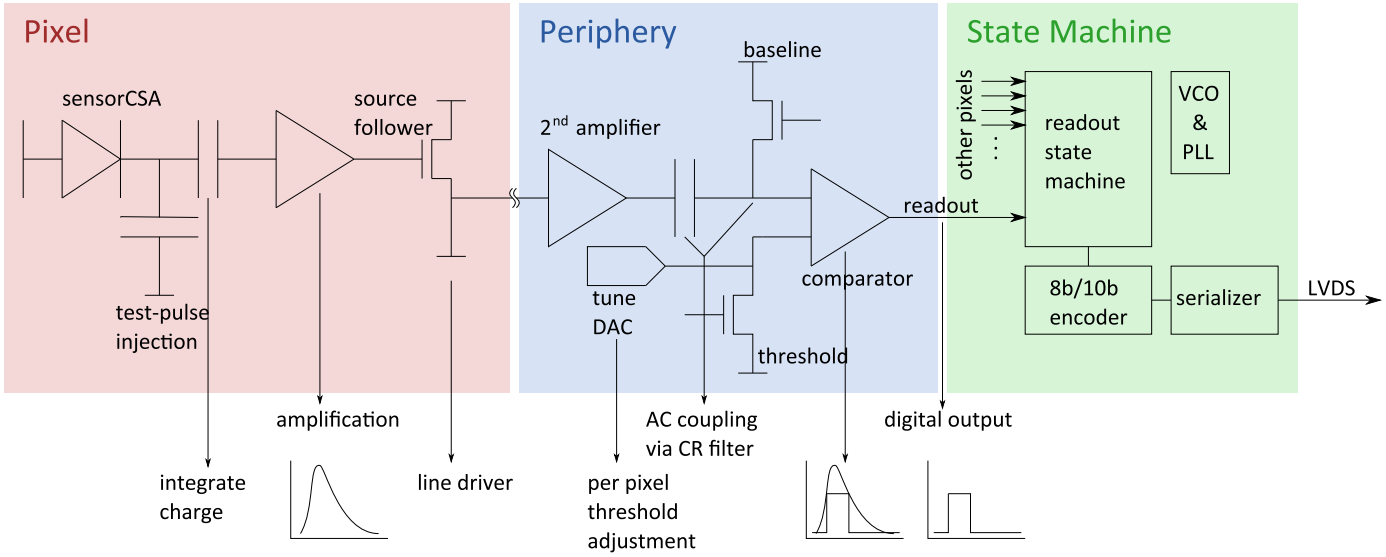

Fig. 3. Block diagram of the signal path in the MuPix7 chip.