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A new cross-detection method for improved energy-resolving photon counting under pulse pile-up

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ABSTRACT

In recent, photon counting detectors (PCDs) have been replacing the energy-integrating detectors in many medical imaging applications due to the formers' high resolution, low noise, and high efficiency. Under a high flux X-ray exposure, however, a superimposition of pulses, i.e., pulse pile-up, frequently occurs due to the finite output pulse width, causing distortions in the energy spectrum as a consequence. Therefore, pulse pile-up is considered as a major constraint in using PCDs for high flux X-ray applications. In this study, a new photon counting method is proposed to minimize degradations in PCD performance due to pulse pile-up. The proposed circuit was incorporated into a pixel with a size of 200×200 μm^2. It was fabricated by using a 1-poly 6-metal 0.18 μm complementary metal–oxide–semiconductor (CMOS) process and had a power consumption of 7.8 μW/pixel. From the result, it was shown that the maximum count rate of the proposed circuit was increased by a factor of 4.7 when compared to that of the conventional circuit at the same pulse width of 700 ns. This implies that the energy spectrum obtained by the proposed circuit is 4.7 times more resistant to distortions than the conventional energy-resolving circuit does under higher X-ray fluxes.

1. Introduction

Photon counting detectors (PCDs) have been widely used particularly in medical X-ray imaging because they could provide higher spatial resolution, signal-to-noise ratio, and detection efficiency such as in X-ray computed tomography (CT) [1–5]. A typical PCD comprises a 2-dimensional array of signal processing pixel circuits and pixel detectors coupled with bump bonding. Pixel detectors in PCDs are typically made of room-temperature semiconductors such as CdTe, CdZnTe and HgI2, etc. [6].

In Recent, PCDs have been improved by incorporating an energy-resolving photon counting (ERPC) circuit, which can measure not only the flux but also the energy spectrum of incident X-rays with only a few energy bins (2–4 bins) [1,4,7–9]. Fig. 1(a) shows an example of an ERPC circuit operation with three energy bins: an e-h pair created by the incident X-ray is amplified through the CSA, which is then compared at three comparators with different threshold voltages. These threshold voltages can be set to define the energy bins.

The final spectrum measured at the pixel detector represents the attenuated information of X-rays from the source to the pixel in-line through an object [10]. Spectral data of the 2-D pixel detectors are then used to synthesize a final image at a specific energy range [11,12]. Other studies reported that summing all spectral data with different weighting factors to each energy bin could generate an X-ray image with an improved contrast-to-noise ratio by up to 90% when compared to that of a simple photon counting (PC) image [13–15].

Nonetheless, a superimposition of pulses in the signal processing unit of each PC pixel, i.e., pulse pile-up, occurs frequently as the X-ray flux increases due to the finite output pulse width of the signal processing unit. Thus, pulse pile-up can induce not only count losses but also distortions in energy spectra in each pixel.

In CT applications, three different approaches are practiced as an attempt to reduce the pulse pile-up effect in ERPCs. The first approach is to reduce the pixel dimension so that the X-ray flux per pixel is reduced [1,8,16]. This approach, however, generates a new problem of enhancing the charge sharing effect and the k-escape peak which can degrade the pixel spectrum and the image quality. The second approach is to reduce the X-ray flux with a filter such as a bow-tie filter [17]. The bow-tie filter is a filter that has a thin thickness at the center and a thick thickness at the periphery. Nevertheless, this can decrease the signal-to-noise ratio (SNR) and induce the beam hardening effect in the spectrum especially at the periphery region of projected data. The third approach is to reduce the CSA output pulse width (CSA-OPW) by using a low value

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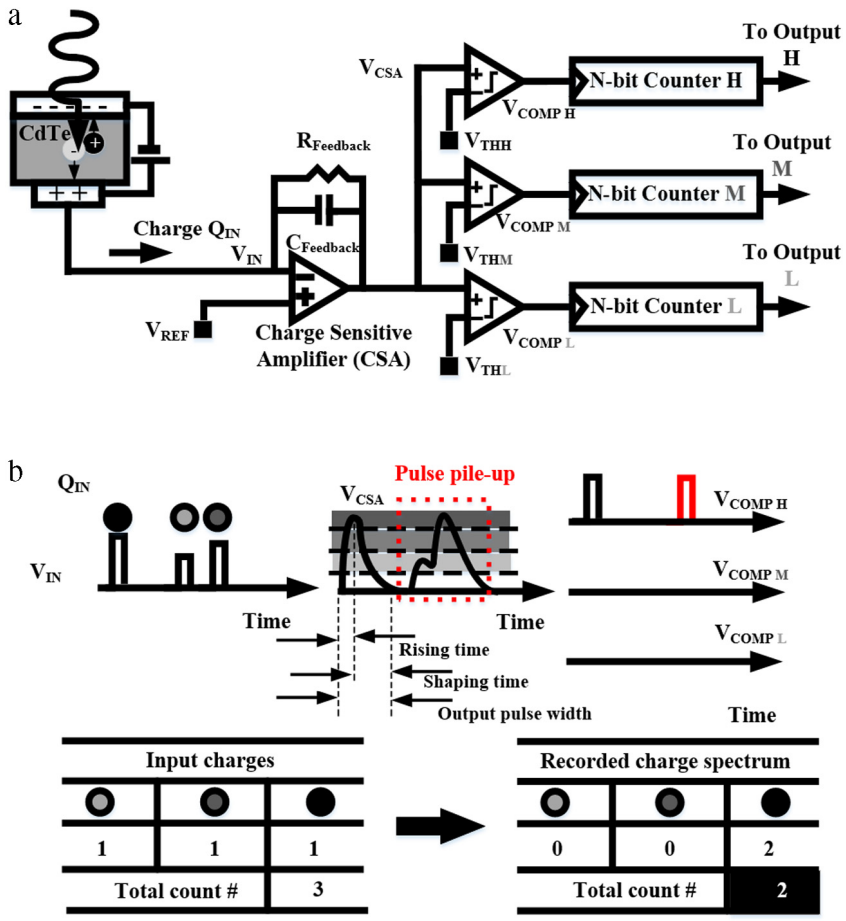

Fig. 1. (a) Circuit topology of an ERPC with three energy bins. (b) Effect due to pulse pile-up in the ERPC circuit; count losses and energy spectrum distortions.

of the feedback resistor, $R_{Feedback}$, in the CSA [8,18]. However, the noise at V_{CSA} is inversely proportional to the feedback resistor value and the charge-to-voltage conversion gain is also decreased as a result. Another disadvantage of reducing CSA-OPW is that it requires fast-operation comparators. Thus, a more sophisticated circuit design with a low noise and a high speed is required, leading to a higher power consumption as a consequence.

In order to minimize these effects, a new PC method that uses a cross detection logic [19] and an energy extraction logic is proposed to find exact energies of photon(s) without shortening the output pulse width. First, the methods used in the proposed CD-ERPC circuit is fully described. Then, the experimental setup to test the CD-ERPC circuit is described in the following section. Moreover, the maximum count rate and the energy spectrum for 90 kVp X-ray with the CD-ERPC circuit are examined in the result and the discussion. Finally, obtained results are summarized in the conclusion.

2. Methods

2.1. Cross-detection ERPC circuit

In order to reduce a count loss and a distortion in an energy spectrum caused by the pulse pile-up effect under high X-ray fluxes, a new CD-ERPC circuit is proposed and its schematic is shown in Fig. 2. In the circuit, two logics are added to a conventional ERPC circuit to model the CD-ERPC circuit; a cross-detection (CD) logic and an energy extraction (EE) logic. The EE logic prevents the distortion in the energy spectrum while the CD logic prevents the count loss due to the pulse pile-up effect.

2.2. Cross detection logic

When a pulse pile-up occurs at the CSA output in a PCD with a single threshold, an event can be lost. As shown in Fig. 3(a), the output of the comparator, V_{COMP}, is triggered only twice for three X-ray inputs.

To avoid such count loss, the CD logic can be added to the PC circuit. The operation of the CD logic is demonstrated in Fig. 3(b). V_{CCSA} is a duplicate signal of V_{CSA} added with an adjustable offset voltage and an adjustable delay. In order to have V_{CD} not be triggered by the electric noise, a positive offset voltage was added to V_{CCSA} because both V_{CSA} and V_{CCSA} were compared at the comparator C in the CD operation. By using different values of widths for the input transistor of amplifier in CD logic, V_{CCSA} with various offset voltages were generated. The offset voltage could be selected among 5, 10, and 15 mV [19].

When the amplitude of V_{CSA} is smaller than the offset voltage, no signal is generated at V_{CD}. In other words, the offset voltage determines the minimum value for detectable energy. Moreover, the offset voltage acts as a threshold for the lowest energy and thus serves as the lowest energy bin for the energy spectrum measurement.

An all-pass filter circuit was used in order to add a delay in V_{CCSA} in the CD logic [20]. The derivation of the phase shift and the transfer function of V_{CCSA} in the all-pass filter are as follows:

$$\text{Phase shift}\,(\Phi) = -2 * \tan^{-1}(2\pi f * R_{Delay} * C_{Delay}) \tag{1}$$

$$\frac{V_{CCSA}}{V_{CSA}} = \frac{1 - S * R_{Delay} * C_{Delay}}{1 + S * R_{Delay} * C_{Delay}} \tag{2}$$

where R_{Delay} and C_{Delay} are the delay resistor and the delay capacitor placed at the positive input of the buffer (Fig. 2). The delay is adjustable by changing R_{Delay} in the CD-ERPC circuit without having a loss in the