Nuclear Instruments and Methods in Physics Research A 867 (2017) 1–6

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Design and characterization of a 64 channels ASIC front-end electronics for high-flux particle beam detectors

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ARTICLE INFO

Article history:
Received 9 November 2016
Received in revised form
30 January 2017
Accepted 16 April 2017
Available online 18 April 2017

Keywords:
Readout electronics
Current-to-frequency converter
Radiotherapy
Hadrontherapy
Charged particles
Ionization chambers

ABSTRACT

A new wide-input range 64-channels current-to-frequency converter ASIC has been developed and characterized for applications in beam monitoring of therapeutic particle beams. This chip, named TERA09, has been designed to extend the input current range, compared to the previous versions of the chip, for dealing with high-flux pulsed beams. A particular care was devoted in achieving a good conversion linearity over a wide bipolar input current range. Using a charge quantum of 200 fC, a linearity within $\pm 2\%$ for an input current range between 3 nA and 12 μA is obtained for individual channels, with a gain spread among the channels of about 3%. By connecting all the 64 channels of the chip to a common input, the current range can be increased 64 times preserving a linearity within $\pm 3\%$ in the range between and 20 μA and 750 μA.

1. Introduction

In radiation therapy, several techniques have been proposed in recent years to achieve a highly conformal delivery of the dose to the tumor target while sparing the healthy tissues. Such techniques require beam monitoring systems providing a fast and precise qualification of the therapeutic beam during the irradiation. These systems are typically composed by sets of parallel plate ionization chambers with different segmentations of the electrodes to provide spatial information.

Since many years, our group has been committed to the development of a family of multi-purpose, multi-channel ASIC chips, called TERA, to read out the charge produced in ionization detectors [1–3]. Tailored for clinical applications, the TERA chips were used in several clinical devices both for quality control in radiotherapy [4] and for beam monitoring in particle therapy facilities [5–7]. They are all based on the recycling integrator principle [8] to convert the input charge into pulse counts, or equivalently the input current into a pulse count frequency, each count corresponding to a fixed quantum of charge. This conversion method offers several advantages as the intrinsic lack of deadtime and the very good linearity up to the maximum conversion frequency. Also, the charge collected at any input channel can be sampled asynchronously with the conversion operations by simply reading the corresponding counter.

The previous version of the chip, TERA08, features 64 channels operating in parallel, each accepting input currents of both polarities and implementing a 32 bits counter with up/down counting capability [3]. TERA08 operates with a clock frequency of 100 MHz and a maximum conversion frequency of 20 MHz. Thus, using a charge quantum of 200 fC, the maximum current that a channel can convert without saturation is about 4 μA. This quantity is well above the typical currents of hundreds of nA measured in the present facilities for particle therapy. However, this limit will be too severe for the pulsed beam structure provided by the next generation of accelerators where, with the aim of reducing the complexity and increasing the performance of the machines, new accelerating technologies are exploited [9–12]. Short beam pulses of 1–10 μs duration with a repetition rate of 1 kHz or less will replace the almost constant beam flux used in the present clinical facilities, leading to an effective beam duty cycle two to three orders of magnitude smaller. Thus, to achieve a similar dose rate, the beam flux in each pulse will increase accordingly.

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http://dx.doi.org/10.1016/j.nima.2017.04.025
0168-9002/

A simple method to increase the current range of the TERA08 was tested recently. It consisted of splitting evenly the input current of a detector element into several readout channels and adding up the counts of these channels to reconstruct the input current. It was shown [13] that this method allows to increase the maximum input current up to 64 times, when all 64 channels are used, preserving the good linearity achieved with the individual channels and with a limited increase in the standard deviation of the measurement. Nevertheless, there are drawbacks with this method; one is the lower number of detector elements which can be read out with a chip, the second is the necessity of reading out the values of a large number of counters, up to 64, and perform their sum. Both affect the versatility of the chip and strongly limit the range of application of TERA08. In addition, a 64 increase in the dynamic range could not be sufficient for the target application.

This paper presents the last version of the chip, named TERA09, designed to overcome these limitations. The charge-to-frequency converter has been improved in order to obtain a larger maximum conversion frequency. Moreover, the chip automatically calculates the partial and total sum of the counter values, which can be directly accessed in dedicated registers. In the design process, special care has been devoted in maintaining as much as possible the backward compatibility such that the new chip can replace the older versions in any of the current devices with small impact on the acquisition system and on the power supply. The results of the tests, presented in the last part of the paper, indicate the possibility to achieve an increase of about two orders of magnitude in dynamic range compared to the TERA08 without a significant loss in sensitivity and linearity, thus adding to this version the additional flexibility to extend its use to high-flux particle beams applications.

2. The TERA09 circuit architecture

Fig. 1 shows the architecture of the chip. It contains 64 identical channels equipped with a current-to-pulse-frequency converter, described in detail later, followed by a 32-bit counter. Currents of both polarities can be converted, leading to increments or decrements of the counters depending on the current polarity.

The readout of the counters can be done independently from the operations of the converters. By asserting a common external *latch* signal the content of all the counters are loaded simultaneously in 32-bit registers. This operation does not stop the activity of the counter, thus there is no dead time due to the readout.

An integrated system of adders triggered by the *latch* signal provides the sum of groups of 4, 16 and 64 channels. These values are stored in additional 34-, 36-, and 38-bit wide registers. Any of these registers can be addressed via seven digital *Channel Select* lines and read out on a 38-bit output bus through a multiplexer. This system allows to read directly the sum of the counters of 4,16 or 64 channels if, in order to increase the dynamic range, the input current is split among the channels, as explained in the previous section.

Particular care has been taken in preventing the overflows of the registers to corrupt the corresponding sums. Indeed, the converter was designed to operate at the maximum conversion frequency of 80 MHz; in this limit condition, the counter 32-bit capacity will be exceeded, and the counter will reset to the starting value, approximately every 50 s. Such a condition is easily identified and corrected for if each individual channel is acquired separately, but may be more difficult to identify and correct when only the sum of a large number of channels is acquired. To identify in advance possible flips of individual counters, an output warning signal *ws* was implemented which is set whenever any of the 64 counters exceeds half of its capacity (see Fig. 1). When such condition occurs, the asynchronous digital *reset_D* can be used to zero all the counters soon after the *latch* signal.

The converter of TERA09 is based on the charge recycling technique and is implemented as shown in Fig. 2.

The input current is integrated over a 1.2 pF capacitor C_{int} via a folded-cascode operational transconductance amplifier (OTA). The output voltage V_A increases when the current exits from the chip (negative current) and vice versa. This voltage is compared with two fixed thresholds, V_{th+} and V_{th-}, by two synchronous comparators. Whenever the comparator input voltage crosses the threshold, the corresponding comparator sets a logic level 1 at one of the input V_B of the pulse generator (PG). When one of its inputs goes high, the PG generates a pulse V_C with a duration of 2 clock cycles that sends a current pulse with polarity opposite to the input current to discharge of the capacitor C_{int}. The pulse adds or subtracts a fixed amount of charge Qc, depending on the outputs of the comparators; this results in a change of voltage across V_A given by Q_C/C_{int}. In parallel, the PG sends an increment or a decrement signal to the counter. The waveforms of these signals are shown in Fig. 3 for the case of a steady negative current.

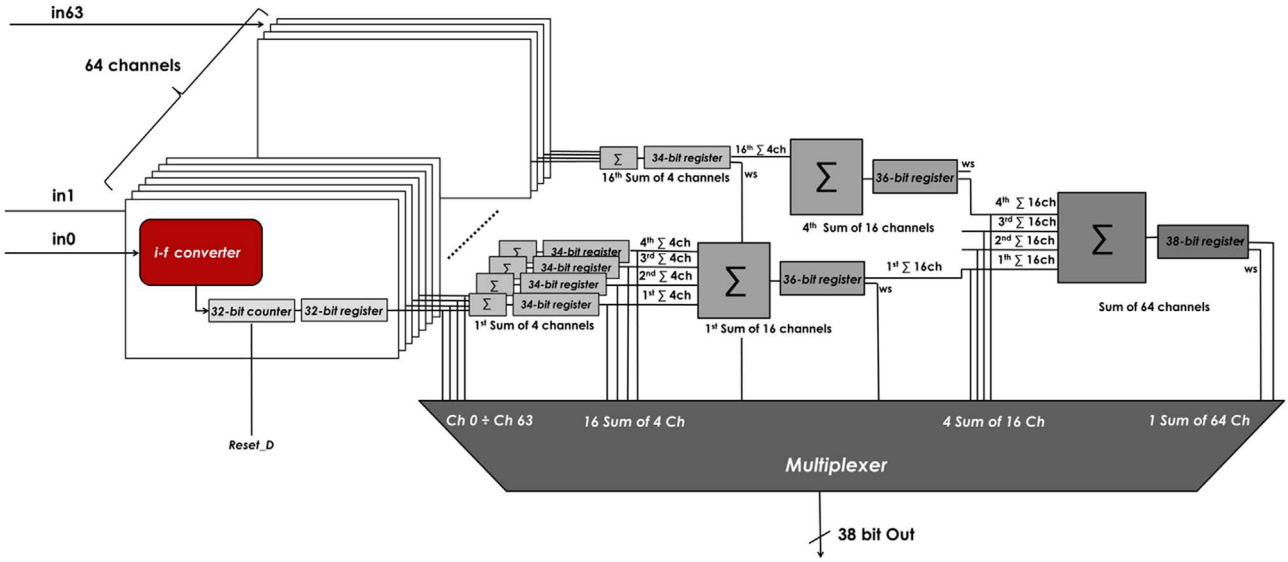

Fig. 1. Block diagram of the TERA09 chip.