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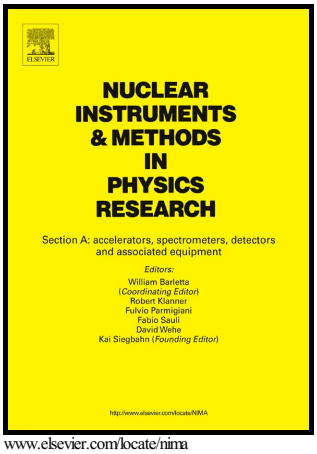

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Exploratory Study of a Novel Low Occupancy Vertex Detector Architecture Based on High Precision Timing for High Luminosity Particle Colliders

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Abstract

Vertex detectors provide space-time coordinates for the traversing charged particle decay products closest to the interaction point. Resolving these increasingly intense particle fluences at high luminosity particle colliders, such as SuperKEKB, is an ever growing challenge. This results in a non-negligible occupancy of the vertex detector using existing low material budget techniques. Consequently, new approaches are being studied that meet the vertexing requirements while lowering the occupancy. In this paper, we introduce a novel vertex detector architecture. Its design relies on an asynchronous digital pixel matrix in combination with a readout based on high precision time-of-flight measurement. Denoted the Timing Vertex Detector (TVD), it consists of a binary pixel array, a transmission line for signal collection, and a readout ASIC. The TVD aims to have a spatial resolution comparable to the existing Belle2 vertex detector. At the same time it offers a reduced occupancy by a factor of ten while decreasing the channel count by almost three orders of magnitude. Consequently, reducing the event size from about 1 $MB/event$ to about 5.9 $kB/event$.

Keywords: Electronic detector readout concepts (solid-state), Front-end electronics for detector readout, Si microstrip and pad detectors.

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