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A parity checker circuit based on microelectromechanical resonator logic elements

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ABSTRACT

Micro/nano-electromechanical resonator based logic computation has attracted significant attention in recent years due to its dynamic mode of operation, ultra-low power consumption, and potential for reprogrammable and reversible computing. Here we demonstrate a 4-bit parity checker circuit by utilizing recently developed logic gates based on MEMS resonators. Toward this, resonance frequencies of shallow arch shaped micro-resonators are electrothermally tuned by the logic inputs to constitute the required logic gates for the proposed parity checker circuit. This study demonstrates that by utilizing MEMS resonator based logic elements, complex digital circuits can be realized.

1. Introduction

Electromechanical computing has attracted significant attention in the past decade driven by the need to replace transistors, as their miniaturization is approaching the physical limits and their energy efficiency is degrading, by smarter multi-function logic elements [1]. With the fabrication capabilities reaching molecular level [2], the notion of mechanical computing has been revitalized and revamped. MEMS/NEMS static switching devices capable of performing multiple logic operations have been demonstrated in the past few years [3–8]. Despite some major advantages, such as cascadebility and ideal leakage properties, these devices have some significant limitations due to contact reliability, contact resistance, surface forces and mechanical delay. To overcome these drawbacks, researchers have been exploring dynamic MEMS/NEMS devices such as micro-resonators as logic elements [9–20], despite their limitations in terms of speed of operation and complexity in building combinational logic circuits. Although there have been successful demonstrations of memory components [9–11], 2-bit logic gates [12–14] and multi-bit logic circuits [14], the realization of complex combinational logics has remained a challenge.

The first demonstration of a dynamic logic, based on a linear NEMS resonator gate, was presented in [12]. The high (low) amplitude response of the resonator at on-resonance (off-resonance) state was defined as the logic output 1 (0). Later, a nonlinear NEMS resonator was used to realize a noise assisted and reprogrammable 2-bit logic device [13]. Mahboob et al. [14] utilized parametric excitation scheme on a single micromechanical resonator to realize a multifunctional logic element to demonstrate 2-bit and multibit complex logic operations. Also, several components of a microcomputer, namely, byte memory, shift-register, and a controlled-NOT gate have been realized in [15] based on the higher order modes of parametrically excited NEMS resonator. Using four coupled, linearly operating nano-resonators, a reversible logic gate, Fredkin gate, has been realized for the first time [18]. Both physical and logical reversibility has been successfully demonstrated. Recently, we have proposed and demonstrated a logic element based on electrothermal resonance frequency tuning of a linearly operated MEMS arch shaped clamped–clamped beam resonator [19]. Although, we have shown all the fundamental 2-bit and basic *n*-bit logic operations, feasibility of building more complex logic circuits based on multiple copies of these logic gates has not been investigated.

The logic parity checker is an essential component for computing systems and information processing chips, in which the accurate matching of all transmitted and received data needs to be verified. To date no attempt has been made to realize this important logic component in the micro/nano-resonator based logic platform. The proposed 4-bit parity checker circuit in this work consists of two *XOR* gates, similar to that proposed in [19], and a differential amplifier to combine the logic outputs of the two *XOR* gates to constitute the final logic output. The parity of the number of logic 1s among the 4 logic inputs is determined and the output signal gives logic state 0 for even parity and 1 for odd parity.

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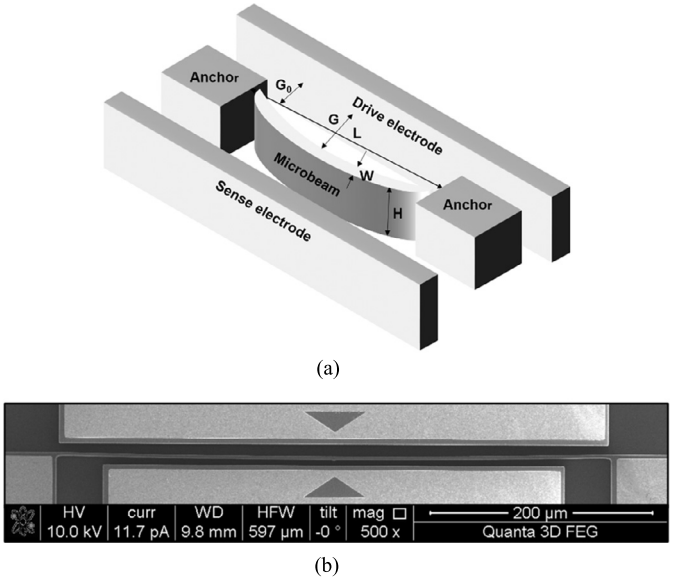

Fig. 1. (a) Schematic of the microbeam resonator, (b) the SEM image of a fabricated device.

2. Implementation and results

Fig. 1(a) and (b) shows a schematic and the SEM image of the fabricated device, respectively. The devices are fabricated on a highly conductive silicon device layer of a silicon on insulator (SOI) wafer by two-mask process [19]. Each device consists of a resonating microbeam and drive and sense electrodes to facilitate electrostatic actuation and capacitive detection. The dimensions of the arch beams are: $L = 500$ µm, $W = 3$ µm, $H = 30$ µm. The gap between the actuating electrode and the microbeam is $G_0 = 8$ µm, at the clamped ends and $G = 11$ µm, at the mid-point due to 3 µm of initial curvature, which is defined by the photo-lithography process to deliberately produce an in-plane arch microbeam.

Fig. 2(a) shows a standard 4-bit parity checker logic block implemented with three *XOR* gates. Fig. 2(b) shows the schematic of the proposed micro-resonator based parity checker circuit. The AC input signal is constantly applied at a fixed frequency and depending on the logic inputs, the logic output, V_{OUT}, is measured across the load resistor, R_L. Note that a high amplitude of V_{OUT} is measured due to a resonance signal, which is defined as the logic output 1 (0).

Fig. 3 shows the experimental setup. Res. X and Res. Y are biased with a single DC source, $V_{DC} = 50$ V. The driving electrodes of the two micro-resonators are provided with the same AC drive signal from the output port of the network analyzer (Agilent E5071C). Res. X output produces $A \oplus B$ logic output whereas Res. Y output produces $C \oplus D$ logic output. The two output signals are subsequently connected to a low noise amplifier (LNA) working in the differential amplifier mode to add and amplify the AC signal. This low noise amplifier (LNA), in its differential amplifier mode, effectively constitutes the third *XOR* gate necessary to complete the logic operation for the proposed parity checker circuit. The final output of the proposed circuit is $P = (A \oplus B) \oplus (C \oplus D)$, which is same as that of a conventional parity checker circuit shown in Fig. 2(a).

The four logic inputs are provided with four different DC voltage sources, V_A, V_B, V_C and V_D, which are connected across the microbeams with series resistors, R_A, R_B, R_C, and R_D, and switches, A, B, C, and D, respectively, as shown in Fig. 3. The logic input 1 (0) is defined by connecting (disconnecting) V_A, V_B, V_C, and V_D from the electrical network by the four switches, A, B, C, and D, respectively. So logic input 1 (0) is represented by the

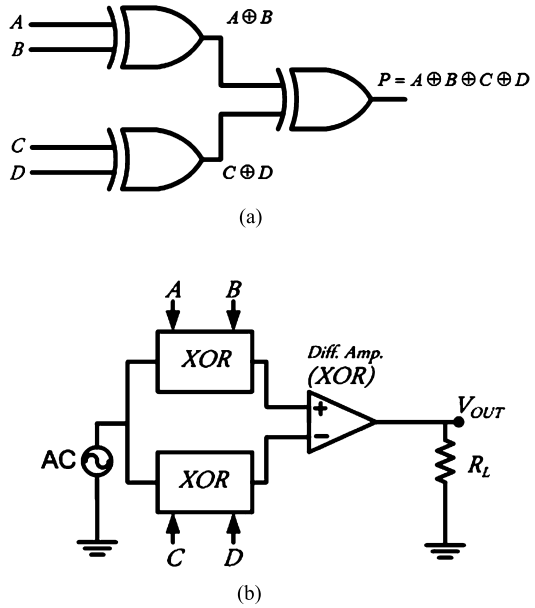

Fig. 2. (a) Schematic of a standard parity checker logic circuit utilizing *XOR* gates. (b) Schematic of the proposed parity checker circuit utilizing microresonator based *XOR* gates. V_{OUT} represents the logic output where a high (low) amplitude corresponds to logic output state 1 (0).

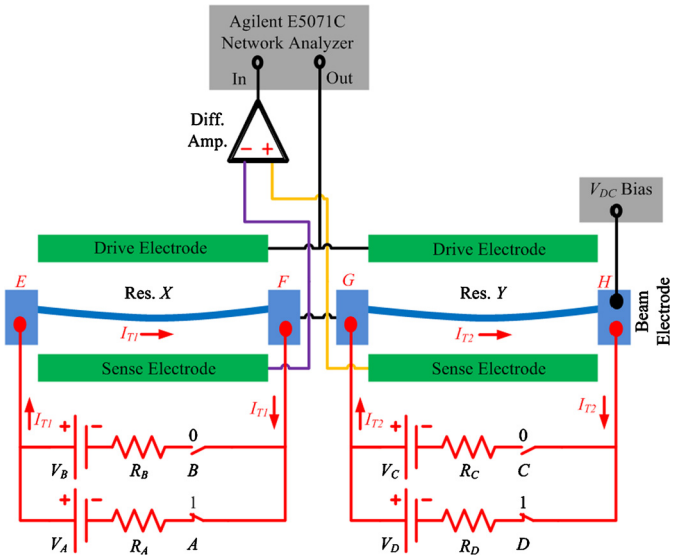

Fig. 3. Experimental setup of the microresonator based 4-bit parity checker circuit. A, B, C, and D logic inputs are represented as switches. Switch ON (OFF) corresponds to logic input 1 (0). Res. X produces $A \oplus B$ and Res. Y produces $C \oplus D$ at the corresponding sense electrodes. Finally, both signals are differentially added by the differential amplifier, which works as the third *XOR* gate to produce the final logic output $P = (A \oplus B) \oplus (C \oplus D)$.

switch ON (OFF) condition for switches A, B, C, and D. The sensing electrodes are used to obtain the output signals from Res. X and Res. Y, which perform $A \oplus B$ and $C \oplus D$ logic operations, respectively. Finally, both of the output signals are differentially added using the LNA to produce the final logic output, P. Note that a high (low) S_{21} transmission signal corresponds to the logic output 1 (0).

We use two similar arch micro-resonators, Res. X and Res. Y with resonance frequencies around 120.95 kHz and 122.42 kHz, respectively. The Res. X and Res. Y microbeams show 110 Ω and 118 Ω resistance, respectively. Note that the difference in the resonance frequencies is due to the fabrication variations in the wafer,