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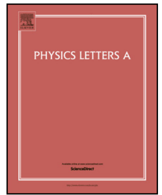

Remarkable charge-trapping performance based in $Zr_{0.5}Hf_{0.5}O_2$ with nanocrystal $Ba_{0.6}Sr_{0.4}TiO_3$ blocking layer for nonvolatile memory device

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ABSTRACT

Two kinds of charge trapping memory device with Au/$Zr_{0.5}Hf_{0.5}O_2$(ZHO)/SiO_2/p-Si and Au/$Ba_{0.6}Sr_{0.4}TiO_3$ (BST)/$Zr_{0.5}Hf_{0.5}O_2$/SiO_2/p-Si structure were fabricated and investigated. The double BST/ZHO films exhibit a larger memory window of 7.36 V under ±14 V sweeping voltages in its C–V curve and the device has good charge retention properties with only small charge loss of ∼5% after more than 10^4 s. The good characteristics are attributed to the inter-diffusion between BST and ZHO where more deep defect sites were created after RTA treatment, which provides high potential barriers for the trapped charges to tunnel back to the silicon substrate. Furthermore, the nanocrystal in the BST layer increases the tunneling barrier of tunneling current into the gate and effectively restrains the leakage of storage charge from blocking layer, which improves the charge retention characteristic.

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Introduction

The charge trapping memory (CTM) devices have been studied for many years, such as silicon-oxide–nitride-oxide–silicon (SONOS) type memory device. CTM as an important component of the nonvolatile flash memories has found many wide applications due to its good endurance and retention, fast program/erase speed and low operating voltage characteristics over the floating-gate devices [1,2]. However, with the further scaling down, few electrons for information storage and low charge trapping efficiency are the crucial problems for nanoscale SONOS devices [3]. To confront the challenge, bandgap-engineered charge trapping layer and high-*k* materials in which oxygen vacancy is thought to be the main defect have been proposed to be used in the CTM devices to obtain a better charge trapping capability and retention characteristics [4, 5].

HfO_2 is considered as the most promising dielectric among the high-*k* dielectrics. It has large band-gap, relatively high dielectric constant (22∼25) and high thermal stability [6,7]. In addition, the electrical properties of HfO_2 can be improved by doping different elements such as Al, Zr and Ta [8,9]. On the other hand, it is well known that ZrO_2 is isomorphous to HfO_2 with a similar structure. And oxygen vacancy is verified as main defect in ZrO_2 and HfO_2 which has been investigated theoretically and experimentally [10, 11]. Furthermore, Zr-doping in HfO_2 can stabilize the tetragonal phase of HfO_2 [12,13], and enhance the *k*-value of HfO_2 [14]. In addition, barium strontium titanate (BST) is a kind of high dielectric coefficient of ferroelectric material, which is widely used in the dynamic random access memory (DRAM) due to its strong nonlinear, small leakage flow, large capacitance rate and anti-fatigue. The dielectric properties of BST film are related to the composition and significantly influenced by the forming process and the annealing process. Therefore, in our case, we investigated the ZHO films with and without nanocrystal BST films as blocking layer to construct CTM devices. We focus on two CTM devices with the structures of Au/ZHO/SiO_2/p-Si and Au/BST/ZHO/SiO_2/p-Si, and the latter shows a distinguished charge-trapping efficiency and a good retention characteristic. And we investigated the microstructure information through high resolved transmission electron microscopy (HRTEM) to make a further study about its charge trapping mechanism.

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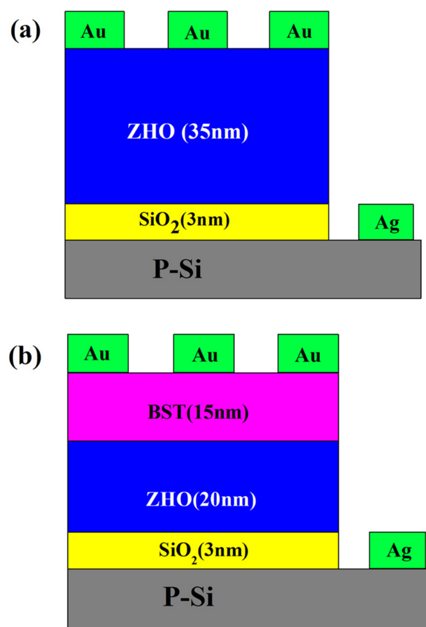

Fig. 1. The schematic structures of memory devices (a) with single ZHO layer and (b) with BST/ZHO double layers.

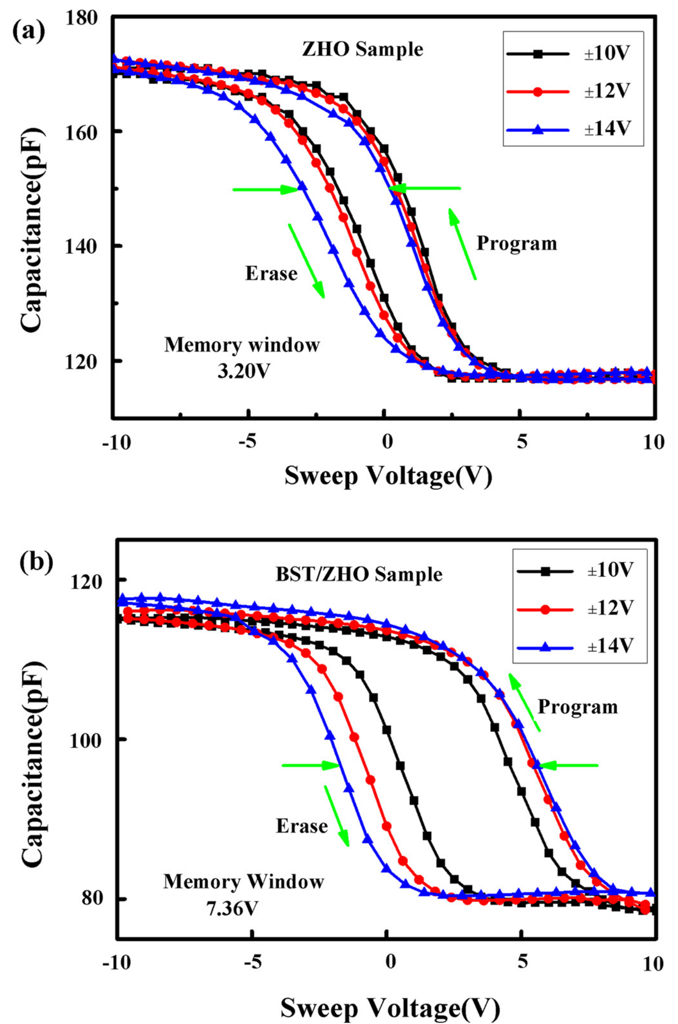

Fig. 2. The typical capacitance–voltage (C–V) curves of memory devices under different sweeping voltages (a) with single ZHO layer and (b) with BST/ZHO layers at 4 MHz.

Experimental details

We fabricated two kinds of CTM structures with Au/ZHO/SiO_2/p-Si and Au/BST/ZHO/SiO_2/p-Si, respectively. P-type (001) silicon wafer with a resistivity of $<0.005\ \Omega$/cm was ultrasonically cleaned in the acetone for 10 min, and then in the alcohol for 10 min, and then in the deionized water for 3 min. After ultrasonic cleaning, the wafer was immersed in HF diluted solution (HF:H_2O = 1:3) for 90 seconds to remove the native oxides. At last, the wafer was cleaned by the deionized water to remove HF, and dried by nitrogen gas gun. The ZHO high-*k* film and BST film were deposited by using RF-magnetron sputtering. The chamber for RF-sputtering was under a mixed ambience of argon and oxygen with the ratio 2:1 at 3 Pa, and the RF power was 80 W. After deposition, the ZHO/SiO_2/p-Si and BST/ZHO/SiO_2/p-Si films were annealed at high temperatures of 600 °C in O_2 atmosphere for 5 min by rapid thermal annealing (RTA). For measuring the electrical properties, dot-shaped Au top electrodes with an area of $\sim 7.47 \times 10^{-4}$ cm^2 were deposited on the surface of the samples using a shadow mask by vacuum evaporation. The electrical properties of the memory structure Au/ZHO/SiO_2/p-Si and Au/BST/ZHO/SiO_2/p-Si were characterized at a high frequency (4 MHz) by using Keithely 4200 semiconductor characterization system.

Results and discussion

The memory device possess a single layer ZHO with a thickness of 35 nm and the double layers 15-nm BST/20-nm ZHO as the blocking layer and the charge trapping layer as schematic diagram in Fig. 1(a) and (b), respectively. The total thicknesses of two kinds of films keep the same. Fig. 2 demonstrates capacitance–voltage (C–V) curves of the samples annealed at 600 °C with different sweeping voltages at a high frequency (4 MHz). It is obvious that the memory windows increase with the increase of the sweeping voltage. ZHO sample shows a largest memory window of 3.2 V when the sweeping gate voltage is ±14 V. However, the memory window of BST/ZHO sample reaches a largest value of 7.36 V at the same voltage, indicating a better charge storage capability. Here, the memory window in C–V curve is defined as the difference of the flat band voltages (V_{fb}) between the program and erase states, which was measured by sweeping the voltage V_G from +14 V to −14 V and then back to +14 V.

To get the microstructure information in BST/ZHO memory device, HRTEM images were shown in Fig. 3. The thicknesses of three functional layers, SiO_2, ZHO and BST, are about 3.50 nm, 21.3 nm and 15.5 nm which well correspond with our designing scheme, respectively. The inter-diffusion at the interface between the blocking layer BST and the trapping layer ZHO could be observed and the thickness of the interface layer is about 6.21 nm as shown Fig. 3(a). The effective inter-diffusion region where additional defect centers could be created during the inter-diffusion process is considered to be the main reason that improves the charge storage capability. So the inter-diffusion phenomenon at the interface BST/ZHO plays a significant role in modifying the charge trapping density in the memory devices. It is also observed that the tunneling layer SiO_2 shows amorphous structure and there is a narrow inter-diffusion region whose thickness is about 1.38 nm at the interface between the tunneling layer and the trapping layer as shown in Fig. 3(b). Just like the SiO_2 tunneling layer, this inter-diffusion region also has a very important role in the charge retention characteristic of the memory devices.

Fig. 3(c) depicts that the blocking layer BST film is well crystallized with random orientations after RTA treatment. It is well seen that there are different nano-grains formations and the crys-

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