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Research and development of a high-performance differential-hybrid charge sensitive preamplifier

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ABSTRACT

A differential-hybrid charge sensitive preamplifier (CSP) was designed by taking a monolithic dual N-Channel Junction Field-effect Transistor (JFET) and a high-speed, low-noise, operational amplifier as the core parts. Input-stage of the circuit employs low-noise differential dual JFET, which ensures high input impedance and low noise. The differential dual transistor makes the quiescent point of the first-stage differential output stable, which is convenient for connecting with the post stage high-speed operational amplifier. Broadband could be amplified by connecting to the double differential dual transistors through the folded cascode-bootstrap. The amplifying circuit which replaces the interstage and post stage discrete components of a traditional CSP with integrated operational amplifier is simpler and more reliable. It simplifies the design of the quiescent point, gives full play to advantages of releasing large open-loop gain, and improves charge-voltage conversion gain stability. Particularly, the charge-voltage conversion gain is larger under a smaller feedback capacitor, thus enabling to gain better signal-noise ratio. The designed CSP was tested, reporting 3.3×10^{13} V/C charge sensitivity, about 90 ns rise time of signals, 35:1 signal-noise ratio to gamma-rays of ^{137}Cs (662 keV) and a 0.023 fC/pF noise slope. Gamma-rays of ^{241}Am (59.5 keV) were measured by the BPX66 detector and the designed CSP under room temperature, providing 1.97% energy resolution.

1. Introduction

During nuclear radiation measurement, preamplification is necessary to provide signal output by the detector to increase the signal-noise ratio, because it has small amplitude and is easy to be influenced by distributed capacitance between the output end of the detector and the input end of the amplifier (Wang et al., 1983; TAFO et al., 2008a; Cicuttin et al., 1997). Currently, a CSP in a high resolution energy spectrum measurement system often uses a single-ended junction JFET as the input-stage and a high-frequency triode as the interstage and post-stage amplifiers. Such a CSP has low noise, simple design, stable gain and good performances (Fiorini et al., 2006; TAFO et al., 2008b; Barbera et al., 1996; Ukibe et al., 1997). However, since it uses a single-ended JFET as the input-stage, the first-stage quiescent point will change with the temperature and bias power. As a result, every stage of amplifier must be designed with a wide operating point. Otherwise, changes of quiescent point will cause output saturation or cutoff when inputting large signals. Moreover, the interstage amplifier composed of traditional discrete components basically adopts a common-base amplification circuit, so open-loop gain often has values of only several thousands. When the feedback capacitor (C_f) is small, the output voltage (V_O) is smaller than Q/C_f, thus decreasing charge-voltage conversion gain and even causing nonlinearity. Hence, a multi-stage triode is often used in the interstage to make a multistage amplifier. This will complicate the circuit structure and make quiescent point debugging more difficult. Fluctuation of the quiescent point will affect the large signal input more significantly. When using an operational amplifier as the interstage amplifier directly under the same single-ended input mode, changes of quiescent point of the single-ended JFET input-stage may make the post stage operational amplifier working at open loop since the operation amplifier adopts differential input mode, finally causing the circuit to turn off. As a result, it is essential to design a circuit with DC feedback to make the quiescent point of a single-ended JFET always consistent with the bias voltage of the operational amplifier. However, this is very difficult. Therefore, this paper used a differential dual JFET based on low-noise and high-transconductance gain as the differential input-stage and adopted a differential output to inhibit fluctuation of the quiescent point. Considering the basically consistent quiescent point of differential output, it could connect to the input-port of the high-speed and low-noise operational amplifier directly. This makes the operational amplifier working under a linear state all the time. In conclusion, the differential-hybrid CSP considering

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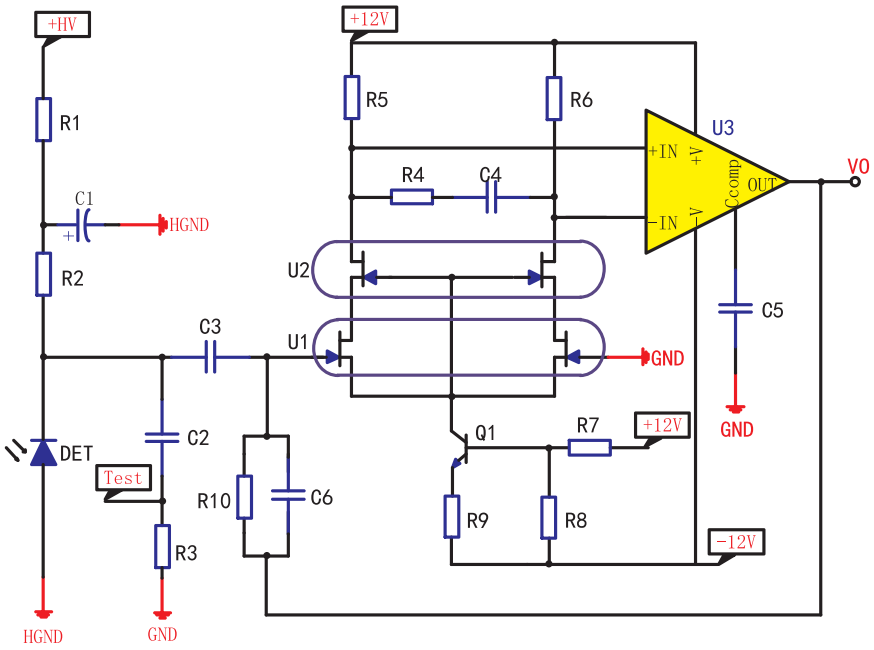

Fig. 1. Circuit diagram of the differential-hybrid CSP.

low-noise input, broadband and high gain is particularly applicable to service environment of high resolution semiconductor detectors like Si-Pin.

2. Circuit design

The circuit of the designed differential-hybrid CSP is shown in Fig. 1. The detector used in the circuit is a BPX66 Si-Pin semiconductor detector. This circuit mainly consists three core parts: input buffer composed of a differential dual JFET, bias circuits composed of a constant current source and resistance, as well as the amplifier-stage circuit composed of an operational amplifier and resistor-capacitor feedback network. Additionally, this detector needs high voltage bias power as power supply, while CSP uses a ± 12 V power supply. The overall working principle of the circuit can be summarized as follows: bias power passes through the first-order RC filter circuit composed of R1 and C1, reducing its noise. The detector will be supplied with bias voltage by connecting bias resistors R2 to the detector. Ionization will occur upon penetration of a X-ray or Gamma-ray into the effective sensitive volume inside the BPX66 detector, which will generate electron-hole pairs that form the signal current under the effect of bias power. The signal current will enter into the input end of the CSP through the coupling capacitor C3. A test signal is connected to the input end of CSP through C2 and R3 for the purpose of index testing. C3 is a coupling capacitor which couples the signal input at the detector or test lead into the input end of U1 and isolate DC voltage of the input end simultaneously to provide a stable quiescent point in the post stage circuit. U1 and U2 are differential dual N-channel JFET. They are connected through a differential folded cascode bootstrapping manner and form the input buffer. Q1 is a NPN bipolar junction transistor (BJT) and forms the constant current source together with R7, R8 and R9 to provide the JFET bias current. U3 is a high-speed operational amplifier. It forms the signal amplifying circuit with R10 and C6 which makes up the resistor-capacitor feedback network. Parts selection and working principles of core components of the circuit are introduced in the following text.

2.1. Input buffer

For CSP, the system noise mainly comes from the input-stage noise. To increase the signal-noise ratio, it shall try to reduce input-stage noise. This could be achieved through parts selection and circuit design. Compared to BJT, MOSFET and MESFET, JFET is superior for lower low-frequency noise and shot noise, smaller input capacitor and stronger shock resistance (Ramírez-Jiménez et al., 2005; Bertuccio et al., 1993; Codino et al., 1996). It is the ideal part for the input buffer. In this paper, the 2SK389 high-performance dual N-channel JFET manufactured by Toshiba was applied. It is characteristic of very low noise, high transconductance, very low input capacitor, high input impedance and small gate leakage current. Parameters are listed in Table 1.

In Fig. 1, U1 and U2 are two groups of the 2SK389 differential dual transistor, which form the differential circuit. Differential connection was employed, so that the input-stage circuit has a high common-mode rejection ratio, thus reducing turbances of power supply noise. Therefore, the input-stage circuit has strong anti-interference. Furthermore, differential connection enables the circuit to decrease the effect of temperature-shift significantly and maintain a stable quiescent point. Meanwhile, since the post stage amplifying circuit uses a differential operational amplifier, the input buffer with differential connection could provide stable differential input signals to the post stage amplifier and protect the post stage amplifier circuit from open loop operation due to changes of the quiescent point (Mathez et al., 2010; Beev and Kiviranta, 2013). U1 and U2 are connected through folded cascode-bootstrap mode. U1 is a common-source connection and U2 is a common-gate connection. Although a common-source circuit has high input impedance, it still has poor frequency characteristics because of the Miller effect. Common-gate circuit has small input impedance, but broad frequency bands. Therefore, a folded cascode amplification circuit could combine advantages of common-source and common-gate connections. It not only maintains high input impedance, but also gains satisfying frequency characteristics (Tong and Hua, 2006). To further improve circuit performance, the gate of U2

Table 1
The key performance parameters of 2SK389.

Characteristic	NF	$\|Y_{fs}\|$	C_{iss}	I_{GSS}
Value	0.5 dB@1 kHz	20mS@I_{DSS} = 3 mA	25pf@1 kHz	−1.0 nA