Chaos, Solitons and Fractals 103 (2017) 555–566

Contents lists available at ScienceDirect

Chaos, Solitons and Fractals

Nonlinear Science, and Nonequilibrium and Complex Phenomena

journal homepage: www.elsevier.com/locate/chaos

Threshold voltage dynamics of chaotic RS flip-Flops

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ARTICLE INFO

Article history:
Received 6 April 2017
Revised 11 July 2017
Accepted 16 July 2017

MSC:
37C05
37C29
37D45
94C05

Keywords:
RS Flip-flop circuit
Minimal model
Neimark–Sacker bifurcation
Chaos
Chaotic strange attractors
Smale horseshoe

ABSTRACT

Chaotic Set/Reset (RS) flip-flop circuits are investigated once again in the context of discrete planar dynamical system models of the threshold voltages, but this time starting with simple bilinear (minimal) component models derived from first principles. The dynamics of the minimal model is described in detail, and shown to exhibit some of the expected properties, but not the chaotic regimes typically found in simulations of physical realizations of chaotic flip-flop circuits. Any electronic physical realization of a chaotic logical circuit must necessarily involve small perturbations from the ideal - usually with large or even nonexistent derivatives in small diameter subsets of the phase space. Therefore, perturbed forms of the minimal model are also analyzed in considerable detail. It is proved that very slightly perturbed minimal models can exhibit chaotic regimes, sometimes associated with chaotic strange attractors, as well as some of the bifurcations present in most of the differential equations models for similar physical circuit realizations. In essence, this work is a mathematical exploration of simple models that reproduce the qualitative behavior of threshold control units of a chaotic RS flip-flop design. It is also shown that this method can be extended to other similar circuits. Validation of the approach developed is provided by some comparisons with (mainly simulated) dynamical results obtained from more traditional investigations.

1. Introduction

Logical circuits are constructed using logic gates representing propositional connectives such as *AND* (conjunction), *OR* (disjunction) and their negation. They, or more precisely physical approximations of ideal logical circuits, have important applications in multiplexers, registers, pseudo-random number generators, quantum network modeling and, in fact, virtually every microprocessor (see, e.g.[3]). Consequently, having efficient methods for analyzing and predicting their behavior, such as by continuous or discrete dynamical systems models is of great value in design, analysis and evaluation.

There are numerous examples of applications for these types of circuits mainly involving chaotic communication and random number generation, such as [17,24]. A well-known example with many applications (including the design of quantum networks [41]) is the RS flip-flop circuit in Fig. 1, which is a feedback circuit comprising two NOR gates (which are negations of OR gates). Note that an OR gate has an output of 1 when at least one of the inputs is 1 and an output of 0 when both inputs are zero, with 1 denoting true and 0 false. An ideal RS*flip-flop circuit* (*RSFF circuit*) is a logical feedback circuit represented in Fig. 1, with input/output behavior described in Table 1, which shows the *set* (S) and *reset* (R) inputs for the circuit consisting of two *NOR gates* with outputs Q and Q'. The input to the output, denoted by $(Q_n, Q'_n) \to (Q_{n+1}, Q'_{n+1})$ may be regarded as the action of a map from the plane $\mathbb{R}^2 := \{(x, y) : x, y \in \mathbb{R}\}$ into itself, where $\mathbb{R}$ denotes the real numbers and in the ideal or perfect case, the coordinates assume the binary values {0, 1}.

The binary input/output behavior, with 0 and 1 representing false and true, respectively, is given in the following table.

We are interested in studying RSFFs designed from Chua's circuit using a threshold control unit [4], such as in Fig. 2. The choice of a NOR implementation of the RSFF comes from the use of only NOR implementations in experiments due to the relative simplicity of construction as opposed to the NAND implementation. The model to be studied in what follows, is more realistic than the one that we formulated and investigated in [2], which was primarily an *ad hoc* construct designed to mimic the known behavior of chaotic flip-flop circuit realizations.

From the discrete dynamical system's perspective, our first goal is to construct the simplest map of the plane (based on bilinear representations of the NOR gates) that models the logical proper-

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http://dx.doi.org/10.1016/j.chaos.2017.07.014
0960-0779/

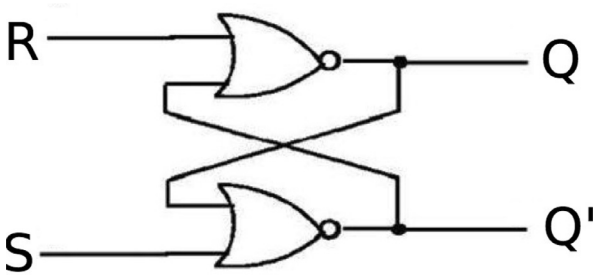

Fig. 1. "Black box" schematic of a NOR gate implementation of a set/reset flip-flop circuit.

Table 1
Binary input/output of $R-S$ flip-flop circuit.

S	R	$S_1 := Q$	$R_1 := Q'$
1	0	1	0
0	1	0	1
1	1	0	0
0	0	1 or 0	0 or 1

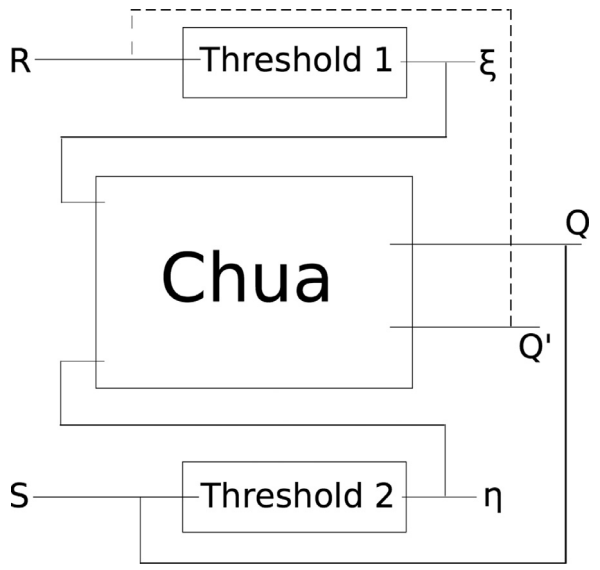

Fig. 2. Chaotic *RS flip-flop* circuit.

ties of the RSFF circuit, with iterates that exhibit most of the interesting properties that follow from basic analysis or have been observed in the dynamics of a variety of physical realizations and their mathematical models. This begs the question of how the dynamics of the planar map models are to be compared with that obtained from simulations of physical realizations of the chaotic RSFF circuit and directly from measurements of its flip-flop relatives and the analysis and simulations of the usual mathematical models, which we shall endeavor to address in what follows.

The usual form of the mathematical models of chaotic logical circuits is traceable back to the pioneering work of Moser [30]; namely, associated three-dimensional systems of piecewise-smooth, first-order, nonlinear autonomous ordinary differential equations (ODEs) obtained from applying Kirchhoff's laws to the realizations. These realizations typically comprise such elements as capacitors, inductors and nonlinear resistors and exhibit highly oscillatory, very unstable and even chaotic dynamics (*metastable operation*), as experimentally observed in physical constructions and SPICE simulations in such studies as [20,21,26], where tunnel diodes of the type used in Chua's circuit (see [4,6,7,32]) are the key ingredients in the construction of the nonlinear resistors. However, nonlinear resistors are not always necessary (*e.g.* [11,39]). There are several connections between the solutions of the model ODEs and iterates of maps that can be used for dynamical comparisons, among which are the following: As observed by Hamill et al. [15], the autonomous nature of the logical circuit equations allows dynamical analysis via the iterates (snapshots) of a fixed time map, which can be reduced to a planar map in special cases as shown in Kacprzak and Albicki [20] and Kacprzak [21]. In addition, the application of a standard explicit one-step integration method is tantamount to the iteration of the map describing the scheme, thus enabling the (approximate) reduction from a continuous to a discrete dynamical system as shown *e.g.* in [8,19]. Of course, there is the well-known method of employing Poincaré sections to analyze three-dimensional continuous dynamical systems using two-dimensional discrete dynamical systems, which has been employed in numerous investigations of chaotic logical circuit realizations such as Feng & Loparo [13], Murali et al. [32], Okazaki et al. [33] and Ruzbehani et al. [37]. In fact, the 1-D Poincaré maps in [13] have features similar to the 1-D reduction of our system to the diagonal. There have also been investigations (such as [27]) where the ODEs are reduced even further to a one-dimensional map.

As it turns out, chaotic logical circuits can be realized using the famous circuit of Chua and its generalizations [6,7], which have depended heavily powerful tools such as Poincaré maps, Melnikov functions and normal forms from the modern theory of dynamical systems and bifurcation theory (see [9,14,19,22,25,34,38,40]) for their analysis. There is also another interesting connection between realization of chaotic logical circuits and nonlinear maps that might afford an opportunity for comparisons with the results obtained from our two-dimensional discrete dynamical system models. This nonlinear map approach has been established in the work of Ditto et al. [12], which features the notion of reconfigurable logic gates comprising connected NOR and NAND gates constructed using one-dimensional discrete dynamical systems and associated thresholds.

Our investigation begins in earnest in Section 2, where we define a (minimal) planar map model of the threshold voltages - derived directly from the ideal RSFF - that plays a foundational role throughout the sequel. Moreover, we derive some basic properties of the minimal map concerning such things as smoothness and the existence and description of an inverse. This is followed in Section 3 with a more thorough analysis of the fixed points of the minimal map - including a local stability analysis and an analysis of stable and unstable manifolds. As a result of this more detailed investigation, we find that the dynamics is quite regular, as expected, when the domain of the map is appropriately restricted. Next, in Section 4 we prove that (one-dimensional) chaos can be generated by localized arbitrarily small C^0 perturbations of the map. For example, it is shown that a tent map can be embedded in a (one-dimensional) stable manifold of a fixed point by such a perturbation, thereby inducing the well-known chaotic tent dynamics. We then prove the existence of several types of more substantial (two-dimensional) chaotic regimes for arbitrarily small localized C^0 perturbations in Section 5. In particular, we show that localized arbitrarily C^0 small perturbations can be fashioned to produce transverse intersections in homoclinic orbits and heteroclinic cycles that generate chaos, horseshoe chaos, multihorseshoe strange chaotic attractors, snap-back repeller chaos and Neimark–Sacker bifurcations. In Section 6, we illustrate our theorems and investigate indicators of chaos and other interesting dynamical properties using numerical simulations of our perturbed models. Finally, in Section 7, we briefly summarize our results, describe some interesting areas of application and discuss a few envisaged plans for related future research.