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Nonlinear dynamics of a class of symmetric lock range DPLLs with an additional derivative control

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ABSTRACT

Nonlinear dynamics of a class of symmetric lock range digital phase-locked loops (SLR-DPLLs) has been investigated using nonlinear dynamical theoretical and computational tools. It has been observed that the system shows a period doubling route to chaos. For certain system parameters the loop exhibits intermittent behavior. The analytical bifurcation analysis shows that inspite of the broader frequency acquisition range than a conventional one the stability of the loop degrades appreciably when the input signal frequency is less than the nominal frequency of the digitally controlled oscillator. The system dynamics have been characterized by measuring the Lyapunov exponent and the correlation dimension. Further it has been shown that the stability range of a SLR-DPLL can be extended using a modified loop filter incorporating time delay feedback technique. The modified SLR-DPLL (MSLR-DPLL) with this additional derivative control along with the loop digital filter (LDF) shows faster convergence than the unmodified one for proper choice of system design parameters. Consequently, the MSLR-DPLL becomes more suitable for practical applications.

1. Introduction:

Digital phase-locked loop (DPLL) is the core part of the modern coherent communication technology. DPLLs find wide application in frequency demodulators, frequency synthesizers, data and clock synchronizer, modems, digital signal processors, hard disk drives, etc. [1]. A DPLL is essentially a discrete time nonlinear closed-loop system that synchronizes the phase of a digitally controlled oscillator (DCO) to the phase of an input signal. The increased application of DPLLs has led to extensive researches to improve its characteristics depending on its various applications. Starting from 1970 different DPLL architectures have been proposed utilizing modified loop structures with regard to specific performances such as extending the lock range or the stable locked zone [2,3], enhancing the speed of the loop [4,5], etc. and analyzed over the years. Among these, a symmetric lock range DPLL (SLR-DPLL) was proposed in [6] to alleviate some problems relating distortions in the demodulated outputs when conventional DPLLs (CDPLLs) are used as frequency demodulators.

For CDPLLs, it has been observed that the distortion produced in the demodulated output signal is due to its asymmetric signal acquisition property. In a CDPLL the time period of the DCO is controlled linearly with the discrete error signal provided by the output of the loop digital filter (LDF), and the controlled DCO frequency is not a linear function of the control signal. Thus for equal amounts of frequency offset of the input signal in the upper side (US) and the lower side (LS) from the DCO nominal frequency (NF) different amounts of the DCO control signal are required to control the DCO time period. This leads to the asymmetric acquisition and tracking behavior of the CDPLL about the DCO NF. To overcome

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this inherent drawback of a CDPLL, i.e., to get symmetrical acquisition as well as tracking response, a simple algorithm for dynamical adjustment of the loop gain was proposed in [6]. According to this algorithm the instantaneous loop gain is modified by the phase error of that instant if the phase error is negative and remains unaltered otherwise. Because of its symmetrical acquisition range, the amplitude distortion of the demodulated output was found to be less in the case of a SLR-DPLL. Thus a SLR-DPLL gives better performance as a FM demodulator (FMD) than a CDPLL.

Although an appreciable number of works regarding the nonlinear dynamics of DPLLs with frequency modulated (FM) input have been reported in the literature [7–9], the nonlinear dynamics of SLR-DPLL has not been explored yet. An idea about the nonlinear behavior of the loop is important for two purposes. Firstly, for the sake of designing an optimum DPLL system and, secondly, to explore the possibility of using DPLLs in chaos based communication systems. To understand the complete behavior of a DPLL we have to resort to the modern nonlinear dynamical tools of bifurcation and chaos theories. In this paper, the nonlinear dynamics of a SLR-DPLL has been studied by bifurcation theory through numerical simulation. It has been observed that the system shows period doubling route to chaos and for certain system parameters it depicts intermittent behavior. The chaotic behavior has been examined by finding the Lyapunov exponent and correlation dimension. A comparative study between a CDPLL and a SLR-DPLL shows that although the dynamical gain control algorithm [6] reduces the distortion in the demodulated output obtained in a CDPLL, an appreciable decrease in the stability range of the loop is found when the input signal frequency is less than or equal to the DCO NF. But in many practical cases, it is desirable that the loop should track signals for high gain values too. For this purpose, the phase error at each sampling instant (SI) has been modified by the difference of the phase errors of two consecutive samples of the input signal. Effectively, the modification using the time delay feedback may be looked upon as the inclusion of a derivative control alongwith the proportional LDF. The present study reveals that the addition of the error controlled signal extends the range of the dynamical stability of the loop. Moreover, the modified system shows faster convergence to the steady state than a CDPLL. These two improved features ensure the enhancement of the application potentiality of the modified SLR-DPLL.

The paper is organized in the following way. Section 2 describes the structure and the system equation of a SLR-DPLL. It presents the analytical bifurcation analysis of the SLR-DPLL. The stability criterion has been derived in this section and a prediction of the route through which the system looses stability is also given. The behavior of the system obtained from numerical simulation studies and the corresponding analysis of the bifurcation phenomena are also included in this section. The chaotic behavior has been quantified by finding nonlinear dynamical measures like Lyapunov exponent and correlation dimension. Section 3 examines the effect of the time delay feedback technique on a SLR-DPLL using analytical and numerical tools. Section 4 summarizes the results of the present study.

2. First-order symmetric lock range digital phase locked loop

2.1. Structure and system equation formulation

The functional block diagram of a SLR-DPLL with multilevel gain is shown in Fig. 1. Let us consider a noise free input signal as

$$s(t) = A_0 \sin[\omega_0 t + \theta_i(t)], \tag{1}$$

where A_0 (Volt) and ω_0 (rad/s) are the amplitude of the input signal and DCO nominal frequency, respectively. $\theta_i(t)$ is the input signal phase given by

$$\theta_i(t) = \Omega t + \theta_0(t), \tag{2}$$

where $\Omega(=\omega-\omega_0)$ is the signal detuning frequency, ω is the input signal frequency signal. $\theta_0(t)$ represents the phase of the input signal. $s(t)$ is sampled by the positive zero crossing edge of the DCO according to the following algorithm [5]:

$$T(k+1) = T - y(k), \tag{3}$$

where $T(=2\pi/\omega_0)$ is the nominal period of the DCO. $T(k+1)[=t(k)-t(k-1)]$ is the time elapsed between $(k-1)$ th and kth sampling instants (SI). $y(k)$ is the DCO control signal at the kth SI $t(k)$.

Considering $t(0)=0$ one can get the kth SI as

$$t(k) = kT - \sum_{0}^{k-1} y(i) \tag{4}$$

The sampler output at the kth instant is written as

$$x(k) = A_0 \sin\phi(k) \tag{5}$$

where $\phi(k)$ is the loop phase error defined as

$$\phi(k) = 2\pi k\xi - \omega_0 \sum_{0}^{k-1} y(i) \tag{6}$$

where $\xi = \omega/\omega_0$ is the normalized input frequency, $y(k) = G_0 x(k)$ is the DCO control signal and G_0 is the gain of the LDF.

We incorporate the dynamical multilevel gain control algorithm, as prescribed in [6], without considering the

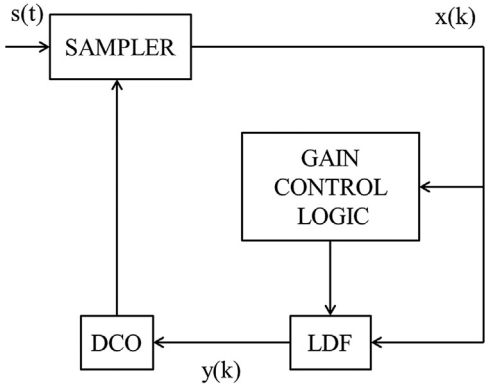

Fig. 1. Block diagram of a SLR-DPLL.