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An energy-efficient SAR ADC using a single-phase clocked dynamic comparator with energy and speed enhanced technique

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Abstract: This paper presents an energy-efficient 500 kS/s 8-bit SAR ADC with a novel dynamic comparator. The proposed dynamic comparator employs a cross-coupling cascode based preamp and an inverter-based pseudo-latch. This approach achieves a 40% higher speed, a 24% lower power consumption, and a similar input-referred noise level, compared with a conventional double-tail dynamic comparator. Moreover, only one single phase clock is required for the proposed comparator. The prototype ADC was fabricated in a 0.5 µm CMOS process with an active area of 0.18 mm^2. Operating under a 1.8 V supply with Nyquist frequency input signal, the ADC consumes 18.2 µW at 500 kS/s and achieves SNDR and SFDR of 47.5 dB and 63.2 dB, respectively. Walden FoM of 188 fJ/conv.-step is achieved.

Keywords: SAR ADCs, asynchronous, dynamic comparator, latch-type comparator, cross coupling, single phase clock

Classification: Integrated circuits

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1 Introduction

A low-power comparator is attractive in energy-efficient successive approximation register (SAR) analog-to-digital converters (ADCs), especially for biomedical applications. Compared with conventional static comparators [1], dynamic comparators [2, 3, 4, 5, 6, 7] are free of static power consumption, which is important to a full dynamic operating SAR ADC. Dynamic comparators also show faster conversion speed than time-domain comparators [8]. However, conventional latch-type sense dynamic comparators [2, 3] confront with voltage headroom issue under a low supply voltage (smaller than two times of threshold voltage). Double-tail latch-type dynamic comparators [4, 5] have less stacking and can therefore operate at lower supply voltages. However, they need two phase triggered clocks, which results in extra power consumption and layout complexity. A single-phase clocked dynamic comparator was presented in [6] to relax clock management. However, the additional loading capacitances at the output of the preamp lead to more power consumption and slower conversion speed.

In this work, we explore a novel single-phase clocked two-stage dynamic comparator with the proposed energy and speed enhanced technique. A cross-

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