An Efficient and Cost Effective FPGA Based Implementation of the Viola-Jones Face Detection Algorithm

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PII: S2468-0672(16)30011-6
DOI: http://dx.doi.org/10.1016/j.ohx.2017.03.002
Reference: OHX 7

To appear in: *HardwareX*

Received Date: 12 September 2016
Revised Date: 17 March 2017
Accepted Date: 25 March 2017

Please cite this article as: P. Irgens, C. Bader, T. Lé, D. Saxena, C. Ababei, An Efficient and Cost Effective FPGA Based Implementation of the Viola-Jones Face Detection Algorithm, *HardwareX* (2017), doi: http://dx.doi.org/10.1016/j.ohx.2017.03.002

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Abstract: *We present an field programmable gate arrays (FPGA) based implementation of the popular Viola-Jones face detection algorithm, which is an essential building block in many applications such as video surveillance and tracking. Our implementation is a complete system level hardware design described in a hardware description language and validated on the affordable DE2-115 evaluation board. Our primary objective is to study the achievable performance with a low-end FPGA chip based implementation. In addition, we release to the public domain the entire project. We hope that this will enable other researchers to easily replicate and compare their results to ours and that it will encourage and facilitate further research and educational ideas in the areas of image processing, computer vision, and advanced digital design and FPGA prototyping.*

Keywords: *Face detection, Viola-Jones algorithm, Field programmable gate arrays, Parallelization, Open source*

1. Introduction.

Field programmable gate arrays (FPGAs) have become extremely popular in virtually all application domains. An example of such an application domain is computer vision, where one often finds object detection and tracking as basic techniques that are used to create more complex systems. The realtime performance of such systems crucially depends on highly efficient and cost effective implementations of those basic techniques. For example, in systems that deal with airport security where one may be interested in object or activity recognition and tracking, face detection is a crucial technique.

One of the most popular face detection algorithms for realtime applications is the Viola-Jones (VJ) algorithm [1]. While other variations of this algorithm have been proposed [2] in this paper, we present a complete hardware implementation of the Viola-Jones face detection algorithm on a low-end FPGA chip. We focus on the Viola-Jones face detection algorithm due to its popularity and efficiency and because it underlies a lot of other face detection algorithms. Our hardware implementation is described entirely in a hardware description language (HDL). We compare our HDL implementation to software based executed on general purpose processors or CPUs. The hardware FPGA based implementation offers a lower performance measured as frames per second (fps) compared to the software CPU-alone implementations for an image size of 320x240 pixels. However, it represents a good solution from a performance-power-price point of view. In addition, the FPGA based implementation has the potential to improve performance if deployed with greater parallelism and especially for larger image sizes on