Colloids and Surfaces A: Physicochem. Eng. Aspects 450 (2014) 156–160

Contents lists available at ScienceDirect

Colloids and Surfaces A: Physicochemical and Engineering Aspects

journal homepage: www.elsevier.com/locate/colsurfa

Preparation of silicon nanowires by *in situ* doping and their electrical properties

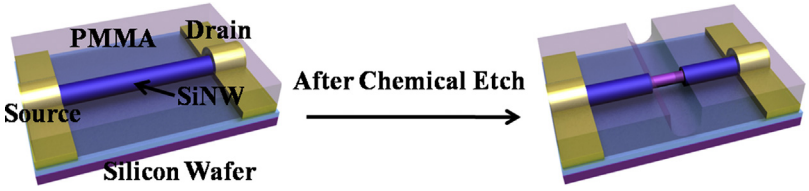
Jindong Wang [a], Gen He [b], Jinwen Qin [b], Lidong Li [a,*], Xuefeng Guo [b,*]

[a] School of Materials Science and Engineering, University of Science and Technology Beijing, Beijing 100083, PR China
[b] Center for Nanochemistry, Beijing National Laboratory for Molecular Sciences (BNLMS), State Key Laboratory for Structural Chemistry of Unstable and Stable Species, College of Chemistry and Molecular Engineering, Peking University, Beijing 100871, PR China

HIGHLIGHTS

- Silicon nanowires were synthesized via low pressure chemical vapor deposition with monodispersed Au catalyst particles.
- The electrical characteristics after chemical etching revealed the radial dopant distribution in SiNWs.
- This system provides a simple method to explore the dopant profile in SiNWs.

GRAPHICAL ABSTRACT



ARTICLE INFO

Article history:
Received 4 January 2014
Received in revised form 5 March 2014
Accepted 9 March 2014
Available online 15 March 2014

Keywords:
Nanowire
Silicon
AFM
Wet chemical etch
Electrical measurement
Dopant

ABSTRACT

Individual silicon nanowires (SiNWs) doped by *in situ* dopant incorporation during growth of the SiNWs was investigated. Electrical charge transport measurements were taken before and after removing the material from the boron-doped SiNW surfaces by wet chemical etching. AFM (atomic force microscopy) images showed the radial cross section of the ~10 nm thick material that was cut off from the SiNW surface. The electrical transport characteristics after each etching cycle revealed the radial core–shell distribution of the activated dopants. The carrier concentration close to the surface of the boron-doped SiNWs was a factor of 6 higher than the value in the core. Using a simple, rapid and reliable technique, the natural distribution of the surface dopants in the SiNWs, which was distinct from many top-down fabricated NWs, explained the enhancement in the charge transport properties of these NWs. This could yield robust properties in ultra-small devices that are often dominated by random dopants fluctuations.

1. Introduction

Silicon nanowires (SiNWs) prepared by Au nanocluster catalyzed vapor–liquid–solid (VLS) growth are one of the most promising building blocks for future nanoelectronic devices, such as transistors, sensors, photodetectors and solar cells [1–6]. For such applications to become commercially viable, large-scale integration of nanowires into devices is required, and uniformity of the electrical properties is critical. It is desirable to understand and be able to control the doping concentration, distribution and activation during the growth process. Some recent research reported some optical and electronic devices were fabricated from organic or inorganic–organic hybrid components also by a doping way [7–10]. In many nanowire growth systems the carrier type majority is controlled by intentional doping. In most cases, the actual dopant concentration, its spatial distribution and the fraction of active dopants is unknown [11,12].

There are few methods that can be used to measure the radial distribution in a single SiNW. Lieber et al. [11] reported a study

* Corresponding authors at: University of Science and Technology Beijing, School of Materials Science and Engineering, Beijing, 100083, PR China.
Tel.: +86 10 82377202; fax: +86 10 82375712/+86 10 62757789.
E-mail addresses: lidong@mater.ustb.edu.cn, lidong@mail.ipc.ac.cn (L. Li), guoxf@pku.edu.cn (X. Guo).

http://dx.doi.org/10.1016/j.colsurfa.2014.03.028
0927-7757/

defining the diameter-dependent location of electrically active dopants in SiNWs prepared using nanoclusters that were catalyzed by vapor–liquid–solid (VLS) growth. The location of the active dopants was assessed with electrical charge transport measurements before and after the controllable thicknesses of the material was removed from the SiNW surface by low-temperature chemical oxidation and etching. This suggested that the surface dopant segregation may be normal for small diameter NWs synthesized with the VLS approach. Rosenwaks et al. [13] used kelvin probe force microscopy (KPFM) to measure the active radial dopant distribution in SiNWs. Their results agreed with previous work where the dopant concentration decreased by almost 2 orders of magnitude from the nanowire surface to its core. Although much progress has been made during past decades, these methods either involve multiple complex steps or they use highly sensitive tools for probes. A simple, rapid and reliable technique needs to be developed to explore the radial dopant distribution of atoms inside SiNWs.

In this paper, micro-nanofabrication technologies for fabricating SiNW field-effect transistors (FETs), followed by high resolution electron beam lithography (EBL) was used to open a small window on the surface of the SiNWs for wet etching to remove the native layer for investigating the radial distribution of dopants through electrical charge transport measurements [11,12]. Comparing with previous reports [11,13–20], this system provides a simple, rapid and reliable method to explore the dopant profile in SiNWs without complex steps or using expensive instruments, which may also be suitable for other nanowire growth systems.

2. Experimental

2.1. Growth of p-type and metallic SiNWs

The nanowire growth procedure used was similar to that reported in previous studies [5,21–24]. Silicon wafers with a 300 nm-thick thermal oxide layer were used as growth substrates and gold nanoparticles with an average diameter of 20 nm (Ted Pella) were used as a catalyst. Boron-doped p-type and metallic SiNWs were synthesized at 460 °C, using 3.9 sccm disilane (Matheson Gas Products, 99.998% purity) as a reactant source. 0.3 sccm diborane (100 ppm, diluted in H_2) was used as the p-type dopant with a B/Si ratio of 1/100,000, 0.6 sccm diborane (100 ppm, diluted in H_2) was used as the metallic dopant with a B/Si ratio of 1/50,000 and 8.9 sccm H_2 was used as a carrier gas.

2.2. Fabrication of silicon nanowire array transistors

High-quality SiNWs were aligned onto APTES ((3-aminopropyl) triethoxysilane))-assembled silicon substrates that had ~1000 nm SiO_2 on the surface, thermally-grown from a PDMS (polydimethylsiloxane)-based microfluidic channel from an ethanol suspension [21–23]. By using another standard lithography technique (BG-401A, China Electronics Technology Group Corporation), windows to individual SiNWs were opened. To form ohmic electrical contacts with metal electrodes [4,5], a buffered HF solution (40% NH_4F:40% HF, 7:1) was used to remove the oxide shell from the nanowires. Metal leads (8 nm Cr followed by 100 nm Au) were then formed through thermal evaporation (ZHD-300, Beijing Technol Science Corporation).

2.3. Device processing

After the SiNW transistors were fabricated, a polymethylmethacrylate (PMMA) layer (950, A4) was spin-cast (4000 RPM, 45 s) onto the surfaces and then baked at 180 °C for 2 min. High resolution electron beam lithography was used along with a design CAD file with a ~5 nm wide line at a specific position, to obtain the window precursor. The resist was developed in a mixture of water and isopropanol (1:3) for the lift-off process, at 4 °C for 1 min with the aid of sonication. After development, the devices were washed in deionized water and dried with a stream of N_2 gas, followed by etching in an oxygen plasma to expose the surface of the SiNWs. The devices then underwent a wet etching process by immersing them into a HF solution buffered with NH_4F (HF (40%):NH_4F (40%) = 1:7) to remove the amorphous SiO_2 layer on the surface of the SiNWs. They were then immersed in a tetramethylammonium hydroxide solution (TMAH, 25 wt%, 60 °C, etch for 2 s) to anisotropically etch the silicon on the surface of the SiNWs.

2.4. Measurements

The morphologies of the SiNW devices were recorded using scanning electron microscopy (SEM, S-4800). Transmission electron microscopy (TEM) was used to study the structural properties of the boron-doped SiNWs. Individual SiNWs were dropped onto a copper grid using a Tecnai F20 high-resolution field emission TEM (HR-FETEM) operating at 200 kV for imaging. In addition, atomic force microscopy (AFM, Nanoscope) was used to characterize single SiNW radical changes before and after the chemical etching processes. After the SiNW transistors were fabricated and the wet chemical etching processes were completed, electrical characterizations were carried out at room temperature in an ambient atmosphere using an Agilent 4155C semiconductor analyzer and a Karl Süss (PM5) manual probe station. Heavily doped Si substrates were used as the global back gate.

3. Results and discussion

P-type silicon nanowires were synthesized via low pressure chemical vapor deposition (CVD) at 460 °C with monodispersed 20 nm Au catalyst particles, comparable to the conditions reported in the literature [3–5,22]. The dopant incorporation efficiency was investigated by adjusting the B_2H_6 and Si_2H_6 flow rates to vary the boron-to-silicon ratio in the inlet gas stream (B:Si) from 1×10^{-5} for p-type semiconductor growth to 2×10^{-5} for p-type metallic growth. SiNWs approximately 30 μm in length were grown from the top of the membrane. They were then released from the surface and suspended in ethanol by sonication, for structural and electrical characterization. TEM was used to study the structural properties of the boron-doped SiNWs. Individual SiNWs were dropped onto a copper grid using a Tecnai F20 high-resolution field emission transmission electron microscope (HR-FETEM) operating at 200 kV, for imaging.

Fig. 1a shows an example of a TEM micrograph collected from an array of SiNWs. The p-type SiNW had a single crystal core structure extending to the outer surface encircled by ~2 nm of amorphous silica. The lattice spacing of 3.17 Å agreed closely with a ⟨1 1 1⟩ growth direction [24,25]. Next, the silicon nanowires were released in ethanol by sonication and were dispersed onto a silicon wafer with a 1000 nm-thick thermal oxide layer through microfluidics [22–24]. Standard UV lithography was then used to define electrical contacts to the individual SiNWs, followed by immersion in a buffered HF etching solution to remove the silica encircling the silicon core. Ohmic electrical contacts were formed with metal electrodes through thermal evaporation before lift-off [4,5].

SEM was used to characterize the structure of the SiNW devices. Fig. 1b shows only one SiNW between the source and drain electrodes, ruling out the possibility of any other SiNWs influencing the electrical measurements. After SiNW transistor fabrication, the electrical characteristics of the transistors were measured at room temperature in an ambient atmosphere using an Agilent 4155C semiconductor analyzer. Heavily doped silicon substrates were