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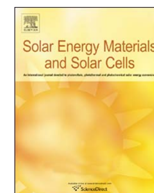

A simple method for pinhole detection in carrier selective POLO-junctions for high efficiency silicon solar cells

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ABSTRACT

Polycrystalline silicon (poly-Si) layers on thin silicon oxide films have received strong research interest as they form excellent carrier selective junctions on crystalline silicon substrates after appropriate thermal processing. Recently, we presented a new method to determine the pinhole density in interfacial oxide films of poly-Si on oxide (POLO)-junctions with excellent electrical properties. The concept of magnification of nanometer-size pinholes in the interfacial oxide by selective etching of the underlying crystalline silicon is used to investigate the influence of annealing temperature on pinhole densities. Eventually, the pinholes are detected by optical microscopy and scanning electron microscopy. We present results on the pinhole density in POLO-junctions with J_0 values as low as 1.4 fA/cm^2. The stability of this method is demonstrated by proving that no new holes are introduced to the oxide during the etching procedure for a wide range of etching times. Finally, we show the applicability to multiple oxide types and thickness values, differently doped poly-Si layers as well as several types of wafer surface morphologies. For wet chemically grown oxides, we verified the existence of pinholes with an areal density of 2×10^7 cm^{-2} even already after annealing at a temperature of 750 °C (lower than the optimum annealing temperature for these junctions).

1. Introduction

Polycrystalline silicon-rich layers on thin silicon oxide films have recently received strong research interest as they form excellent carrier selective junctions on crystalline silicon substrates after appropriate thermal processing. The excellent passivation properties combined with a low specific contact resistance [1–3] have translated into solar cell efficiencies of 25.3% using the tunnel oxide passivated contact (TOPCon)-approach for one carrier polarity [4] and 25.0% with poly-Si on oxide (POLO)-junctions for both carrier polarities [5].

Since their first application to silicon bipolar junction transistors the carrier selective current transport across the POLO-junctions has been widely investigated [6,7]. An explanation based on localized carrier transport through pinholes in the interfacial oxide has been proposed [8,9] complementary to direct tunnelling for very thin oxide thickness. The break-up of the interfacial oxide film under annealing has been identified as a crucial process step in the formation of high quality junctions [10–12]. Recently, small regions showing direct contact between the crystalline silicon and the poly-Si layer were found in transmission electron microscopy (TEM) investigations of POLO-junctions with excellent passivation properties [13]. From the TEM results a diameter of 5 nm was obtained for these regions and their density was estimated to be about 1×10^8 cm^{-2}. Both values are in agreement with the proposed pinhole model [8,9].

While TEM is the best choice to determine the diameter of pinholes in the 5 nm range, it only allows a rough estimation of their density for values below 10^9 cm^{-2}. Plus, it is hard to find pinholes at all [13]. Thus, a complementary method to determine the pinhole density is required. A step in this direction was undertaken using conductive atomic force microscopy (C-AFM) [14]. However, this method is limited by the lateral conductivity of the poly-Si films, which has to be small in order to enable the required resolution. Recently we developed a new concept, which circumvents the constraints of TEM and C-AFM by combining selective etching with tetramethylammonium hydroxide (TMAH) and simple optical microscopy (OM) [15]. After a proof of concept experiment using lithographically patterned samples [15] this

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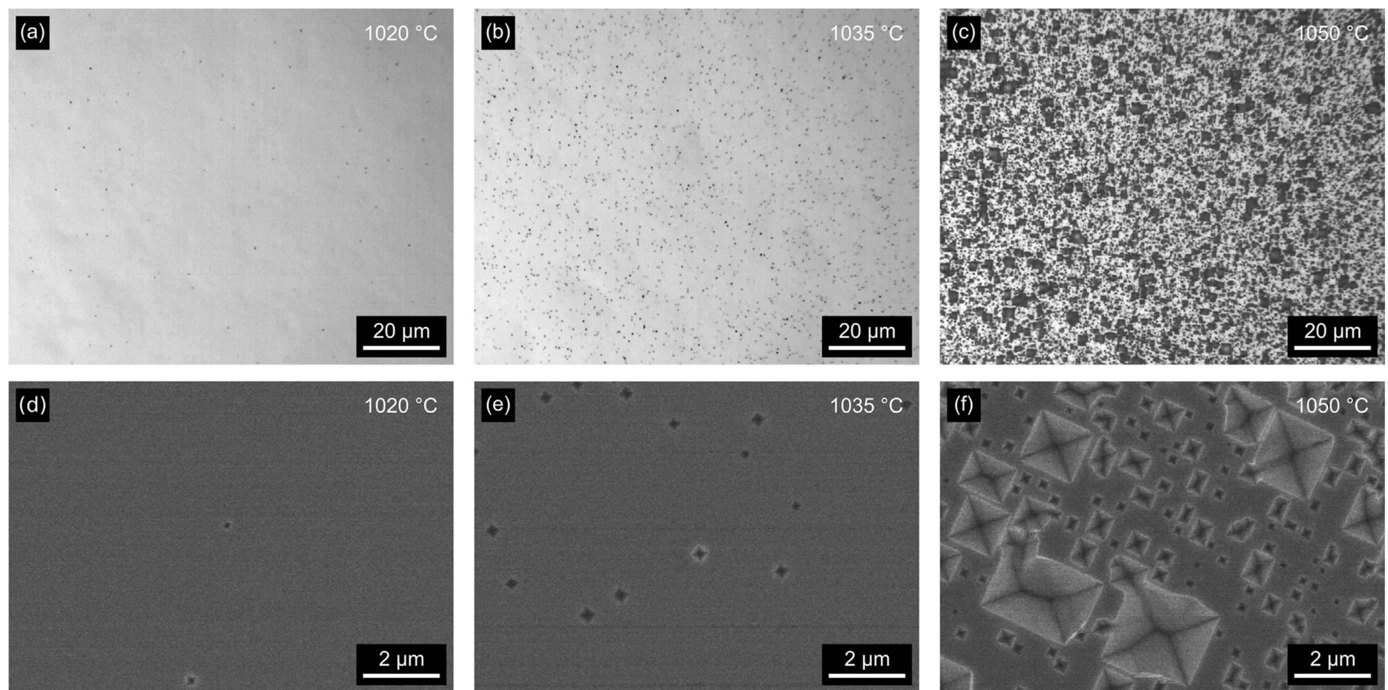

Fig. 1. OM ((a)-(c)) and SEM ((d)-(f)) images after etching of wafers annealed at 1020 °C ((a), (d)), 1035 °C ((b), (e)), and 1050 °C ((c), (f)), respectively. Etch pits are clearly visible with both methods. SEM reveals typical inverted pyramid structure.

method was recently applied to POLO-junctions correlating the pinhole density in interfacial oxide films with their excellent saturation current density and contact resistivity [16].

In this paper, we investigate the influence of annealing temperature on the pinhole density in POLO-junctions with J_0 values as low as 1.4 fA/cm^2. We study extensively the stability of the undercutting procedure to ensure that no additionally holes are generated during the etching process. Finally, we apply this method to several different substrates, oxide types and thickness values as well as differently doped poly-Si layers to demonstrate the versatility of this method.

2. Experimental

POLO-junctions were prepared on planar, shiny-etched 90 Ωcm *p*-type 290 µm-thick FZ wafers. A ~2.1 nm silicon oxide film (thickness determined by ellipsometry) was grown by dry thermal oxidation. Then a 120 nm-thick *n*-type poly-Si layer was produced by LPCVD and subsequent phosphorus ion implantation. After junction formation for 60 min in N_2 ambient at different temperatures (1020 °C, 1035 °C, and 1050 °C) J_0 values were extracted from photoconductance decay measurements.

To identify pinholes in the oxide by OM, the poly-Si layer has to be completely removed while the oxide should remain as is. This was achieved by removal of the native oxide formed on the poly-Si layer using hydrofluoric acid (HF) solution and subsequent selective etching in 15% TMAH solution at 80 °C. Overetching leads to an undercut of the oxide. The resulting etch pits in the underlying silicon are much larger than the original pinholes. So, they can readily be detected. To verify the stability of the etching process, each wafer was split into several pieces and etched for different times (120 – 360 s). Pinhole densities were counted from OM images and correlated to scanning electron microscopy (SEM) images.

3. Results and discussion

3.1. Influence of annealing temperature

The saturation current densities for the samples annealed at 1020 °C and 1035 °C are 1.4 fA/cm^2 and 1.5 fA/cm^2, respectively. A further increase of annealing temperature to 1050 °C leads to a much higher J_0 value of 55 fA/cm^2. This dramatic change is accompanied by the increase of pinhole density within the oxide. Massive dopant diffusion from the poly-Si layer into the crystalline silicon could also increase the saturation current due to related Auger recombination. However, previous reports show that the fraction of Auger recombination remains small compared to recombination at the crystalline Si/SiO_2 interface [1,17].

After etching 1.5×1.5 cm^2 small pieces of the samples in 15% TMAH solution at 80 °C for 240 s, the dependence of pinhole density on annealing temperature can directly be seen in the OM images in Fig. 1(a)-(c). The average areal etch pit density (EPD) increases from (a) 5.9×10^5 cm^{-2} at 1020 °C to (b) 1.3×10^7 cm^{-2} at 1035 °C while J_0 remains constant. In the framework of the model in Ref. [9], both samples possibly represent a regime, in which the pinhole area fraction is that low that the total surface recombination is dominated by the recombination in the regions with still intact interface oxide. The average EPD after annealing at (c) 1050 °C of 1.1×10^8 cm^{-2} is accompanied by a significant increase in J_0. The reader should note that these J_0 values are determined by a QSSPC measurement in the center of the wafer, which corresponds to an average over several cm^2. Local inhomogeneities on a smaller length scale are not resolved in this measurement.

In Fig. 1(d)-(f) corresponding SEM images are shown, revealing the typical inverted pyramid structure resulting from anisotropic etching of (111) and (001) planes by TMAH. For the wafer annealed at 1020 °C single etch pits with 150 nm up to 170 nm edge lengths are found. The maximum structure size increases with temperature to 480 nm after annealing at 1035 °C and up to 2.5 µm after annealing at 1050 °C (only counting not overlapping etch pits). The latter two samples also show smaller etch pits. The percentage of structures with sizes below 125 nm increases from 0% (1020 °C) to 12.6% (1035 °C) up to 23.5% (1050 °C). This indicates the augmented formation of new holes within the oxide with increasing temperature. At the same time, holes grow larger at higher temperatures. As reported before [16], the EPD observed by SEM is slightly higher in comparison to values obtained from OM. This is due to the resolution limit of optical microscopes. Nevertheless, the SEM

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