



Recombination-free reactive ion etch for high efficiency silicon solar cells



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ABSTRACT

Carrier lifetime degradation of reactive ion etch-processed silicon samples are investigated. Two types of carrier recombination: reversible and irreversible degradations induced by reactive ion etching (RIE) are identified. Irreversible carrier recombination is due to surface damage created by the RIE process that propagates a few microns deep into the silicon substrate. Reversible carrier recombination, on the other hand, is found to be caused by radiation damage when RIE etches only into the silicon oxide, and nitrogen annealing can restore the degraded carrier lifetime. A recombination-free RIE process is then developed in combination with a passivation stack consisting of silicon dioxide and silicon nitride layers. This improved RIE process is applied to the development of high efficiency silicon solar cells resulting in a conversion efficiency exceeding 24%.

1. Background

Reactive ion etch (RIE) is widely used in microfabrication and micromachining due to its highly directional etch capability, ability to transfer lithographically patterned complicated features to the underlying layers, lack of dangerous wet chemicals, cleanliness, and compatibility with vacuum-based fabrication processes. [1–3]. It has been extensively used in the fabrication of nanopores in silicon [4], memory devices [5], multilevel interconnect Si devices [6], photonic crystals [7,8], three-dimensional micro- and nanostructures [9] and micro-electromechanical systems [10]. The benefits of RIE have been realized in the photovoltaic (PV) industry as well, particularly in the area of surface texturing to enhance light absorption and improve the solar cell performance. Traditionally, wet chemicals containing alkaline and acidic solutions are used to create pyramidal textured [11] and honeycomb shaped structures [12] to increase the light absorption. However, the large amount of silicon removed (~20 μm per side) during the texturing and surface damage etch by wet chemical processes poses a significant challenge when PV manufacturers move toward thin crystalline silicon solar cells. Compared to wet chemical process, RIE offers several advantageous: compatibility with thin crystalline silicon solar cells [13], independence of crystallographic orientation [14], and very low reflectivity on the textured surface [15]. Advances in RIE have been concentrated into the development of surface texture to further reduce the front surface reflectance. One of the significant attributes emerged from the RIE is the black silicon surface texture, which greatly modifies the silicon into needle-shaped surface structures resulting in very low reflectivity and high absorption of the light in the blue response region [16]. Black silicon structures have been applied in the development of

high efficiency laboratory [17] and industrial silicon solar cells [14,15]. Despite those benefits, RIE generates defects near the surface of the semiconductor [18,19], consequently degrading the electrical performance of solar cells and other devices [20–25]. Defects and increased recombination induced by the RIE has limited the high efficiency potential of silicon solar cells, with only a handful groups demonstrated the incorporation of RIE into the development of silicon solar cells [25–29]. This contribution presents types of carrier lifetime degradation induced by RIE process and techniques to reverse the degradation. In addition, a novel technique was developed to circumvent the lifetime degradation induced by RIE in the process of etching the dielectric and passivation layers. Finally, this technique has been applied in a chain of high efficiency silicon solar cells developments achieving the conversion efficiency higher than 24%.

2. Experimental details

RIE was performed in an Oxford PlasmaLab80 system using CHF₃ plasma with the addition of O₂. The process pressure was 55 mTorr and the total gas flow rate was kept constant at 55 SCCM (cubic centimetre per minute at STP). Samples were placed on the water-cooled (25 °C) bottom electrode that was powered by a 13.56 MHz RF generator. The parallel upper and lower electrodes are 240 mm in diameter. The RF powers reported are forward powers, as the measured reflected power was insignificant. The RF power of 200 W and the dc bias of 450 V were used in this study. P-type float zone < 100 > 100 mm diameter low resistivity (1–5 Ωcm) silicon wafers were used in the experiments. Silicon dioxide (SiO₂) and silicon nitride (SiN_x) was grown in thermal oxidation and low pressure chemical vapor deposition (LPCVD)

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furnaces. Oxidation was done at 1000 °C for 30 min, followed by nitrogen anneal at the same temperature for 30 min. In the SiN_x deposition, the reactant gases – dichlorosilane (SiCl₂H₂) and ammonia (NH₃) were introduced into one end of a furnace tube, and pumped out from the other end. Deposition temperature and process pressure were maintained at 787 °C and 450 mTorr during the operation. Prior to the dielectric passivation of SiO₂ and SiO₂/SiN_x stack, samples were etch-polished, cleaved into quarter-piece samples and cleaned in RCA SC1 and SC2, followed by etching the samples in dilute HF (10%) to make the sample surface hydrophobic. The samples were then either thermally oxidised or grown in the LPCVD furnace, followed by forming gas annealing (FGA) in 10% hydrogen in nitrogen at 400 °C for 30 mins. Effective carrier lifetime was measured at an injection level of 10¹⁴–10¹⁵ carriers per cm³ using the quasi steady state photo-conductance decay (QSSPCD) technique based on Kane and Swanson technique, assuming an intrinsic carrier concentration of n_i = 8.95 × 10⁹ cm⁻³ (at 297 K). Carrier lifetime represents bulk and surface recombination. Thickness of the SiO₂ and SiN_x films were measured by the filmetrics based on the spectral reflectance technique that analyses the reflected light perpendicular to the films. In the interests of experimental simplicity and clarity, no surface phosphorus diffusion (to suppress surface recombination) was used. Surface conditions of samples before and after RIE process were also measured and analysed by scanning electron microscopy (SEM). The RIE etch rate on Si (38 nm/min) was determined by first creating the mesas etch pattern, and then measuring the etch depth of mesas etch pattern by the alpha-step stylus profilometer; while that for SiO₂ (44 nm/min) and SiN_x (62 nm/min) was by the filmetrics before and after RIE.

3. Results and discussion

3.1. Reactive ion etching into silicon

RCA cleaned silicon samples were oxidised, annealed in FGA, and then etched by RIE at 200 W for 6 min. The RIE etch process time of 6 min was sufficient to remove all of the oxide and to etch a fraction of silicon. After etching into the silicon, all samples were again cleaned in RCA solutions and re-passivated by thermal oxidation. Effective carrier lifetime of samples was measured before and after RIE. Substantial lifetime degradation was observed for post-RIE etched samples and the degraded lifetime could not be recovered by subsequent FGAs (see Fig. 1). Fig. 2 further shows SEM pictures of samples before and after RIE process, and post-RIE samples were associated with significant

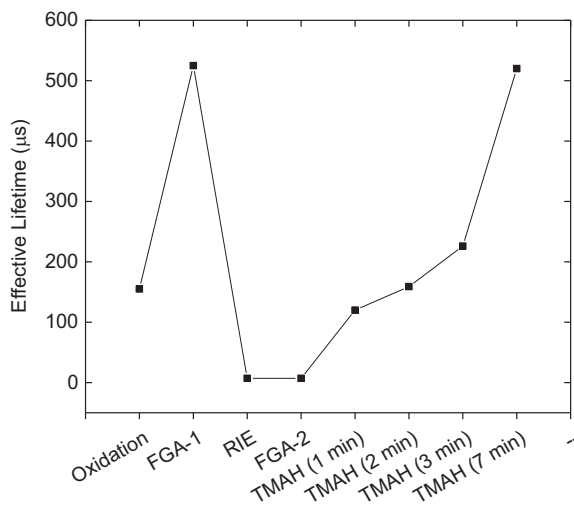


Fig. 1. Lifetime of samples after different process conditions. Carrier lifetime measurements were undertaken at the carrier injection of 1×10^{15} cm⁻³, except for RIE and FGA-2 that were measured at 1×10^{14} cm⁻³.

surface damages. These surface damages have been caused by the energetic ion bombardment during RIE process, consequently resulting in recombination-active defective surface. The passivation oxide of these RIE-processed sample was stripped in dilute HF, and then etched in TMAH (Tetramethylammonium hydroxide) at 90 °C for varying times. Approximately 0.3–0.4 μm of silicon per minute is removed in 10% TMAH at 90 °C. After etching in TMAH, the samples were cleaned in RCA solutions and re-passivated with SiO₂, followed by annealing in FGA. The aim of this work was to understand whether the RIE-induced damage is shallow or deep within the silicon. The fractional recovery of sample lifetime by etching in TMAH for 3 min is approximately 40%. A restoration of pre-RIE lifetime was achieved by increasing the TMAH etch time up to 7 min, which etched about 2–3 μm of silicon. The possible cause of RIE-induced damage propagating a few microns deep into the silicon substrate is explained by the cumulative lattice damage under the semiconductor surface caused by the continuous ion-bombardment during RIE [30,31]. Wet chemical etch could recover the degraded lifetime, however, it negates some benefits of RIE such as etch anisotropy and is undesirable if the solar cell fabrication is at the final stage.

3.2. Reactive ion etching into SiO₂

For the next set of RCA cleaned SiO₂ passivated samples the etch time of RIE was kept sufficiently short to etch only the SiO₂ layer, while avoiding to etch into the silicon. A wide variety of RF power (100 W and 200 W) and time (30 s and 60 s) were used for those samples. Lifetime degradation was still observed for all samples, although the degradation was considerably less than in the case where the RIE etch penetrates the oxide into the silicon. However, degraded lifetime of SiO₂ passivated samples where RIE enters the SiO₂ layer only was recovered to pre-RIE condition, following the FGA anneal (see Fig. 3). The similar recovery is observed by the nitrogen (N₂) annealing. The phenomenon of effective carrier lifetime recovery could be related to radiation damage. References have shown that radiation induced by plasmas generates trapping sites in oxide layers when exposed to RIE [32]. So long as the RIE etch does not penetrate into the silicon, the loss of the lifetime can be recovered by annealing in FGA or N₂. Rapid thermal anneal in N₂ ambient was also able to recover the degraded lifetime of SiO₂ passivated samples.

3.3. Reactive ion etching into SiN_x

SiN_x was further explored for RIE process. It was observed that when SiN_x was grown directly on the silicon the carrier lifetime was much lower than that grown with SiO₂. The cause of this has been due to the generation of defects in the silicon, induced by the mismatch in coefficients of thermal expansion between silicon and silicon nitride, together with its high extent of intrinsic stress, which may influence the carrier lifetime in the underlying silicon as well as the electron mobility [33]. Inserting a thin SiO₂ layer between SiN_x and the silicon provides a comparable or better passivation quality as SiO₂ grown sample [34]. Samples grown with a stack of SiO₂ (~20 nm) and SiN_x (~60 nm) were etched in RIE for 58 s. Note that ramp up and gas pressure stabilization steps during the RIE etch also remove a nanometer or two of SiN_x. The etch time was designed in a way to leave SiN_x with a thickness of 2 nm or less, without etching on a thin layer of SiO₂. In addition, a silicon shadow mask having a fractional exposure (i.e. 1%, 10% and 100%) was also used during the RIE process. The purpose of the shadow mask is to (1) identify if there is a varied degree of lifetime degradation exists with respect to the fractional exposure, and (2) if limiting the RIE exposure to SiN_x would be necessary to mitigate the degradation. Fig. 4 shows the lifetime of SiN_x coated samples before and after RIE. As shown in the Fig. 4, pre- and post-RIE processed SiN_x coated samples were observed with negligible change in carrier lifetime for different degrees of fractional exposure. The reason for this could have been that

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