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Silicon heterojunction interdigitated back-contact solar cells bonded to glass with efficiency > 21%

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ABSTRACT

Previously, IMEC proposed the i^2-module concept which allows to process silicon heterojunction interdigitated back-contact (SHJ-IBC) cells on thin (< 50 μm) Si wafers at module level. This concept includes the bonding of the thin wafer early on to the module cover glass, which delivers mechanical support to the wafer and thus significantly improves the production yield. In this work, we test silicone and ethylene vinyl acetate bonding agents and prove them to be resistant to all rear side processes, including wet and plasma processes. Moreover, a lift-off process using a sacrificial SiOx layer has been developed for emitter patterning to replace conventional lithography. The optimized process steps are demonstrated by the fabrication of SHJ-IBC cells on 6-inch 190 μm-thick wafers. Efficiencies up to 22.6% have been achieved on reference freestanding wafers. Excellent V_{oc} of 734 mv and J_{sc} of 40.8 mA/cm^2 lead to an efficiency of 21.7% on silicone-bonded cells, where the high V_{oc} indicates the process compatibility of the bonding agent. The developments that enabled such achievements and the key factors that limit the device performance are discussed in this paper.

1. Introduction

According to the silicon wafer-based photovoltaic roadmap, Si raw material cost accounts for approximately 61% of the current solar cell price [1] and 30–40% of the total module cost [2]. Hence, to reduce the Si consumption, fabrication of solar cells on thin (< 50 μm) monocrystalline Si wafers, with as little kerf-loss as possible, is being studied by several groups [3–6]. However, such thin wafers are much more mechanically fragile than standard ~180-μm-thick wafers, which are widely used today on production lines [1]. To reduce wafer breakage and achieve high industrial production yield, proper industrial handling techniques of thin wafers are essential [7]. One possible approach is to mechanically support the thin wafer with rigid carriers during wafer transport and cell processing [8–12]. This is the case for the integrated interconnect-module (i^2-module) concept, proposed by IMEC [13]. The process starts with thick, highly p+ doped Czochralski wafers. A micron-thick porous Si layer is formed at the top of the wafer by electrochemical porosification [14]. Then, monocrystalline Si foils are epitaxially grown on top of the porosified wafers [15]. After epitaxy, the cell processing starts by first processing the front sides of the foils while the foils remain attached to their parent substrates. Then the thin foils are detached and bonded to a module glass superstrate using an adhesive. The rear sides of the foils are now accessible and are processed to finalize the solar cells at the module level. In this way, the thin foils are mechanically supported during most of the processing steps and foil breakage can be significantly reduced, without extra bonding cost.

In the i^2-module concept, certain constraints are imposed to the cell process, particularly due to the bonding. For instance, the bonding agent used for gluing the foil to glass limits the temperature budget of the rear side process to typically 300 °C [16]. This motivated us to select low-temperature (< 250 °C) amorphous silicon (a-Si:H) for rear side passivation and junction formation (e.g. back surface field (BSF), emitter). The potential of a-Si:H/c-Si heterojunction (SHJ) contacts was demonstrated at device level by Panasonic [17] and further substantiated recently by introducing the interdigitated back-contacted

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(IBC) architecture [18,19], Based on the SHJ-IBC technology, the world's record Si solar cell with an efficiency as high as 26.3% was recently reported by Kaneka [20].

In this study, we report the recent progress in the process development of SHJ-IBC solar cells bonded to glass. A lift-off method using a sacrificial SiO_x layer was implemented for emitter patterning to replace the conventional lithography and etching used in the past [21,22]. In the first part of this paper, these process developments and the resulting cell design and fabrication process are described. Functional cells were achieved on freestanding and bonded n-type float zone (FZ) wafers. Two different bonding adhesives, which are also applied as encapsulants in standard Si solar cell modules, silicone and ethylene vinyl acetate (EVA), were evaluated at cell level. In the second part, the results of these cells are discussed in detail. The factors limiting the cell performance and the main losses of the cells are identified.

2. Experimental details

2.1. Solar cell design and fabrication process

All cells, with an active area of 4 cm^2, were processed on 190-µm thick n-type FZ wafers (6 in., < 100 > , 3 Ω cm). The wafers were first exposed to a H_2SO_4:H_2O_2 (4:1) mixture for 10 min to remove organic contamination remaining on the surface, followed with rinsing in deionized water and a 2 min treatment in diluted HF:HCl:H_2O (2:5:93). Spin drying was used to complete the cleaning sequence. A thermal oxide layer (~34 nm) was grown on both sides of the wafers at 975 °C for 40 min. The front side was exposed to vapor HF to remove the oxide and then the wafers were textured in a 25% tetramethyl ammonium hydroxide (TMAH) based solution at 80 °C for 20 min, which resulted in approximately 10% reflectance @700 nm at the front side. As shown in Fig. 1, a-Si:H and subsequent SiN_x depositions were performed using radio frequency plasma-enhanced chemical vapor deposition (RF-PECVD) in a parallel plate AK1000 Inline system of microsystems for the front passivation and antireflection coating, respectively. Then the wafers were split into two groups depending on the bonding agents. One group was manually bonded to Corning's EAGLE XG® Slim Glass using silicone encapsulant. We have reported previously that plasma-silicone interaction during a-Si:H deposition has a detrimental impact on passivation quality [23]. For this reason, an Ar plasma treatment was utilized to form a more densely crosslinked layer by local modification of the exposed silicone surface [23]. The other group was manually glued to identical glass using EVA. Diluted TMAH (1:12 in water, 5 min, 35 °C) and HCl:H_2O_2:H_2O solution (1:1:5, 10 min, 20 °C) were used for the post-bonding cleaning. Finally, the wafers were dipped in HF:HCl:H_2O (1:1:20, 1 min, 20 °C). Then, the i/n+ a-Si:H layer (~32 nm) and SiO_x/a-Si:H stack (~630 nm/~26 nm) were deposited using RF-PECVD. This SiO_x layer is a sacrificial mask for the subsequent lift-off process. Photolithography and wet etching were used to define the BSF area. The emitter area was passivated by i/p+ a-Si:H (~16 nm) and patterned by a self-aligned lift-off process, which was carried out in diluted HF:HCl:H_2O (2:1:20). A stack of 120 nm-thick indium-doped tin-oxide (ITO) and 3 µm-thick Cu was deposited using Leybold A600 system and Pfeiffer e-gun PLS 580 system followed by lithography patterning to form the rear side metal contact. Thermal annealing at temperatures below 200 °C was applied to the finished cells using BTU's VMCA belt furnace in order to improve the contact behavior (Fig. 2). Identical cells were also fabricated on freestanding wafers without bonding to glass to investigate the influence of the presence of boding agents and glass on the cell performance.

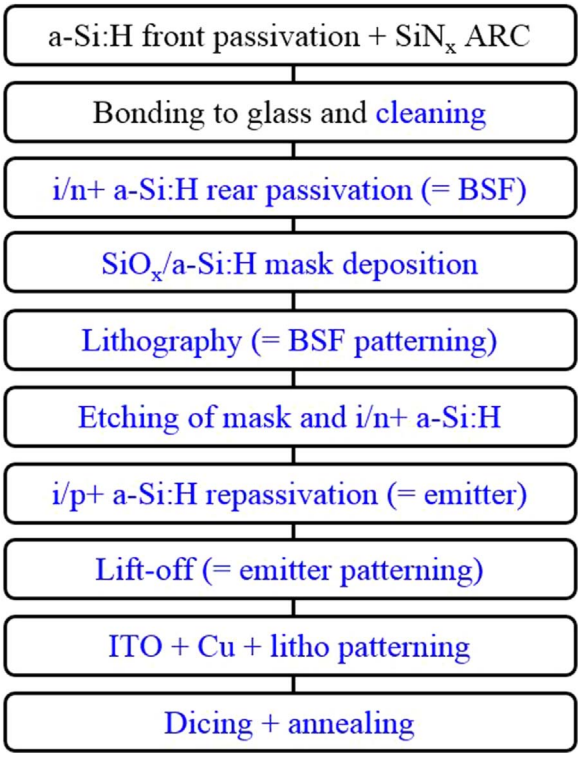

Fig. 1. Integration process flow of SHJ-IBC cells on bonded wafers used in this work [25]. All the rear side process steps (in blue text) are performed in presence of bonding agent.

Analysis methods include photoluminescence (PL) imaging, quasi steady state photo-conductance (QSSPC), dark and light I-V, spectral response, and Suns-V_{oc} measurements. The I-V characteristics of all cells were measured at different incident light intensities ranging from dark to 1 sun and with an mask implicating a designated illumination area of 3.97 cm^2. The series resistance R_s was determined from the Bowden method [24]. The shunt resistance R_{shunt} and saturation current density J_{02} were determined from Suns-V_{oc} measurements. The values of R_s, R_{shunt}, and J_{02} used to calculate FF loss were also confirmed by additional fitting of dark I-V curve using a two-diode model [26]. The reflectance and external quantum efficiency (EQE) were measured on the same position for some of the best cells from each split. The pseudo fill factor (pFF), saturation current density J_{01}, and lifetime of finished cells were extracted from Suns-V_{oc} measurements.

2.2. Rear side patterning approach

The back contact scheme results in additional fabrication complexity mainly due to the presence of interdigitated n- and p-type a-Si:H strips. Although photolithography is widely used for patterning on laboratory scale, it is a costly technique and thus not useable for large-scale production. In addition, the photoresist can introduce contamination during emitter patterning, which may affect both carrier transport and passivation quality at the a-Si:H/c-Si heterointerface [27]. This is particularly true for our bonded cells, as it is difficult to completely remove the photoresist on the bonding agent (e.g. silicone)

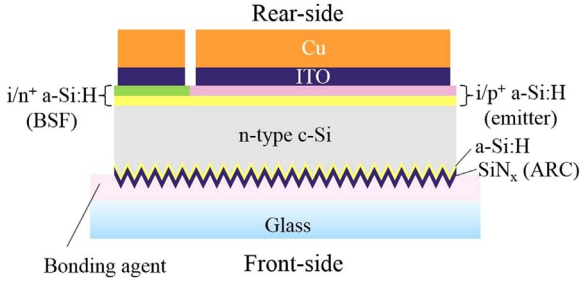

Fig. 2. Schematic of the bonded SHJ-IBC solar cell architecture (not drawn to scale).