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Development of ZnO nanowire based CdTe thin film solar cells

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ABSTRACT

This work reports on the development of CdTe thin film solar cells grown on ZnO nanowire arrays. The focus was placed on utilising ZnO nanowire arrays as a replacement to the conventional ZnO thin film buffer layer, thereby requiring minimal alteration to the existing solar cell structure. Incorporation of nanowires was found to alter subsequent film growth and processing, with the nanowire dimensions changing device performance significantly. Shorter, ~100 nm, wires were found to produce particularly low device performance of < 0.5% whilst longer wires in the range 250–2000 nm were able to produce more functional cells. Working devices of up to 9.5% efficiency were achieved through the production of "embedded tip" nanowire solar cells. Variation of the nanowires length demonstrated that the nanowires were involved in carrier recombination and that this may be the performance limiting factor.

1. Introduction

Nanowires (NW) have attracted a great amount of interest for implementation in a range of electronic and opto-electronic devices [1,2]. By constraining carrier transport in two dimensions this allows carriers to be directed via the remaining unconstrained dimension. The NW arrays offer the potential for improved charge carrier mobility and reduced reflection, allowing improved optical collection [3]. For photovoltaics (PV) this has obvious benefits [1] but the implementation of nanowires in real solar cells is challenging. Whilst high efficiencies are often demonstrated for single nanowire devices [4,5], realisation of nanowire cells on a macroscopic scale is more difficult. Due to the high aspect ratio of nanowires, and the often challenging nature of their growth, their use adds an extra layer of complexity to already tricky solar cell fabrication processes. For CdTe solar cells the preferred implementation would be to grow CdTe nanowires and produce cells via the "core-shell" approach [6]. In this design the CdTe wires are coated with *n*-type CdS and transparent conductive oxide (TCO) layers to form a continuous *p-n* junction across the whole device, theoretically improving collection and reduce carrier recombination in the CdTe layer. There are a number of issues with this design however. Firstly it requires the CdTe solar cell to be grown in the inverted "substrate" geometry [7] (rather than more established "superstrate" geometry) which is lower efficiency and commonly results in back contacting issues [8]. Additionally growth of CdTe NWs is via the vapour-liquid-solid (VLS) mechanism which requires a catalyst layer such as gold [6], or bismuth [9], may generate related impurity deep levels [10] and thus increase recombination within the CdTe. There is also often the need for a CdTe thin film under-layer to be used for growth [6], in which case some of the NW enhancement may be compromised due to recombination in the thin film layer.

An alternative approach is to use a material which is more easily deposited as a NW than CdTe as the basis for NW incorporation. Whilst some authors have attempted this by using CdS nanopillars coupled to a CdTe thin film [11], this too requires the VLS growth route and thus the inclusion of Au seed layers. In contrast ZnO nanowires may be grown easily via low-temperature, self-assembly electrochemical deposition, without the requirement for contaminating seed layers [12]. The incorporation of ZnO nanocones as a replacement for the CdS layer has previously been reported [13], but these devices demonstrated very low conversion efficiency of < 3.2% as may be expected due to the inherently poor quality of the ZnO/CdTe junction [14]. Here we take a different approach by simply maintaining ZnO in its usual implementation. ZnO films are commonly included in a number of thin film PV technologies such as CdTe or $CuIn_xGa_{1-x}Se_2$ (CIGS) as what is typically referred to as a resistive "buffer" layer [15], located between the n-type window layer and the TCO front contact. This layer serves to improve device performance as it allows the window layer, typically CdS, to be reduced in thickness without any loss of device performance. Optimising the thickness of the resistive buffer layer requires a trade-off between the benefits yielded by the layer and the additional series resistance it produces. For example a relatively thick buffer layer >

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500 nm may block shunting pathways and improve band alignments, but the overall performance could decrease due to resistive losses. The use of nanowires as the buffer layer should allow nanowire lengths greater than the equivalent film thickness to be utilised. This serves to the same purpose as the planar buffer layer, but without hindering current transport across the junction. It may also generate a physical separation between the CdTe layer and front contact, making front to back contacting shorting extremely difficult. This is in addition to the inherent light trapping properties of the nanowires which should allow this nanowire buffer layer to play a dual role.

This paper reports on the development of CdTe solar cells of up to 9.5% efficiency incorporating ZnO NWs deposited by a low temperature electrochemical deposition route. The respective challenges for production as well as electrical and optical properties of NW and planar equivalent cells will be discussed.

2. Materials and methods

2.1. ZnO nanowire deposition

ZnO NW arrays of varying dimensions were electrodeposited on FTO-coated glass substrates which had a 100 nm ZnO film deposited on the surface by RF sputtering. NWs were produced by the reduction of dissolved molecular oxygen in zinc chloride aqueous solutions [16]. In particular, 5×10^{-4} M $ZnCl_2$ (> 98.0%), 0.1 or 2 M KCl (> 99.5%) ultrapure aqueous solutions, saturated with bubbled oxygen, were used. The KCl concentration was varied (i.e. 0.1 and 2 M) in order to tailor the nanowire growth mechanism [15]. The nanowire length was varied by modifying the charge density applied during the electrodeposition.

2.2. Solar cell fabrication

CdS layers were deposited at 200 °C by RF sputtering at a power of 60 W and with a thickness of ~200 nm. ~4 μm thick CdTe layers were then deposited via close space sublimation (CSS) under 25 Torr of nitrogen using source and substrate temperatures of 605 °C and 510 °C respectively. A 30 s nitric-phosphoric (NP) acid etch was carried out prior to post-growth chloride activation treatment to enhance the Cl in-diffusion [17]. The $CdCl_2$ (or for later samples $MgCl_2$ [18]) activation step was performed in air in the range 410–450 °C and 20–40 min, the time and temperature being optimised for different sample structures. Following this the samples were etched in NP solution for a further 15 s prior to application of a matrix of gold back contacts deposited by thermal evaporation.

2.3. Thin film and device characterisation

The cross sections of the ZnO nanowire arrays and solar cells were analysed using an ULTRA plus ZEISS field emission scanning electron microscope (FESEM). For focussed ion beam (FIB) milling a FEI Helios Nano Lab 600 Dual Beam system, equipped with a focused 30 kW Ga liquid metal ion source was used. Samples were then transferred to a Hitachi SU70 SEM from imaging and electron beam induced current (EBIC) analysis via a Matelect ISM5 specimen current amplifier set to a 10 nA measurement range. Beam conditions used for EBIC analysis were 5 kV with a beam current of 0.9 nA. Optical reflectance measurements were performed using a Shimadzu Solidspec 3700 spectrophotometer with an integrating sphere. Complete cell characterisation was carried out using a Bentham PVE300 system for external quantum efficiency (EQE) measurements, an AM1.5 calibrated TS space systems solar simulator for current voltage (*JV*) analysis and a Solatron SI1260 impedance analyser for capacitance voltage (*CV*) measurements.

3. Results

3.1. Initial test samples

For initial device testing samples were produced utilising a range of nanowire dimensions and growth conditions to assess the most suitable configuration. CdTe and CdS deposition parameters were kept identical to that for deposition on typical ZnO films, however it was anticipated this was likely to be non-optimal for the ZnO NW solar cells due to variations in film growth rates on the different surfaces. Three NW array types were initially compared as shown in Fig. 1a: i) “short” ~100 nm NWs, ii) “long type I” ~1 μm NWs with growth condition I and iii) “long type II” ~1 μm NWs with growth condition II. The difference between the I and II NW array type is the growth conditions. For II NW array type, growth along the radial direction (i.e. lateral growth [19]), which thickens the NWs, was intentionally promoted. In contrast, for I NW array type growth occurs primarily along the longitudinal direction of the NW. For comparison a 100 nm thick ZnO film buffer layer with no NW coating was used for a control device. Complete solar cell structures were deposited as described in the experimental section using each of the substrate types. These initial test devices were $CdCl_2$ treated using standard cell processing conditions (25 min at 410 °C) for typical planar devices with ZnO thin films. Gold back contacts used for the purpose of these initial test cells were small dot contacts of 2 mm diameter. EQE and *JV* analysis of each device was then carried out with curves for the highest efficiency contacts shown in Fig. 1b and c respectively. It is important to note that for test contacts of this size determined J_{sc} values from *JV* curves are often overestimate due to the problem of edge collection effects from the dot contacts. Because the back surface has been NP etched and is thus slightly tellurium-rich, the area of the contact is effectively extended and thus the J_{sc} is typically overestimated however V_{OC} and *FF* are unaffected. This is a common problem when small area contacts are used. Hence for this initial set of test devices we are only using a comparative analysis rather than quoting absolute J_{sc} or efficiency values.

Initial device testing showed that cell performance was dramatically reduced by the incorporation of NW arrays. The peak efficiency decreased from > 11% with a V_{OC} of 0.80 V for the planar cells to < 2.4% for all NW cells with a peak *Voc* of 0.46 V, and other performance parameters, *FF* and J_{sc}, similarly degraded. While none of the NW samples performed well the 1 μm type II NW array based device (< 2.4%, 0.46 V) was significantly better than the 100 nm NW (< 1.2%, 0.38 V) and particularly that based on 1 μm type I NW array (< 0.5%, 0.22 V). *JV* curves (Fig. 1c) imply an overall reduction in the quality of the junction for NW devices, while EQE curves (Fig. 1b) give some indication of the cause. The overall EQE response is reduced for the nanowire samples, corroborating the lower J_{sc} values. It is notable however that for the ZnO film device there is a distinct drop in EQE below the CdS band edge (~520 nm). For the ZnO nanowire based devices there is little discrepancy in performance above or below the CdS band edge, indicating that for the NW cells the CdS thickness is almost negligible. There are three possible explanations for this outcome either; i) the CdS growth rate is significantly reduced on NW arrays resulting in a decreased as-grown film thickness, ii) CdS/CdTe inter-diffusion is greatly increased due to the increased surface roughness or iii) re-evaporation of CdS occurs during CdTe deposition due to the increased surface area of the films. As CdS was clearly visible following sputtering deposition on the NWs and optical transmission measurements confirmed its presence, the CdS layer must be primarily lost during CdTe deposition. Enhanced CdS/CdTe inter-diffusion rather than re-evaporation from the surface seems the most probable mechanism given the sublimation temperature of CdS exceeds that of CdTe. This loss of CdS is likely to have significantly contributed to the reduced device performance as ZnO/CdTe junctions are of much lower