Solar Energy Materials & Solar Cells 158 (2016) 2–10

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Passivating electron contact based on highly crystalline nanostructured silicon oxide layers for silicon solar cells

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ARTICLE INFO

Article history:
Received 31 March 2016
Received in revised form
6 June 2016
Accepted 16 June 2016
Available online 9 July 2016

Keywords:
Surface passivation
Passivating contact
Nanostructure
Silicon oxide
Nanocrystalline
Microcrystalline
Poly-silicon
Crystallization
Raman
Transmission line measurement
Phosphorous diffusion

ABSTRACT

We present a novel passivating contact structure based on a nanostructured silicon-based layer. Traditional poly-Si junctions feature excellent junction characteristics but their optical absorption induces current losses when applied to the solar cell front side. Targeting enhanced transparency, the poly-Si layer is replaced with a mixed-phase silicon oxide/silicon layer. This mixed-phase layer consists of an amorphous SiO_x matrix with incorporated Si filaments connecting one side of the layer to the other, and is referred to as nanocrystalline silicon oxide (nc-SiO_x) layer. We investigate passivation quality, measured as saturation current density, and nanostructural changes, characterized by Raman spectroscopy and transmission electron microscopy, carefully studying the influence of annealing dwell temperature. Excellent surface passivation on n-type and also p-type wafers is shown. An optimum annealing temperature of 950 °C is found, resulting in a saturation current density of 8.8 fA cm^{-2} and 11.0 fA cm^{-2} for n-type and p-type wafers, respectively. Even before forming gas annealing, emitter saturation current densities of 27.9 fA cm^{-2} (n+/n junction) and 32.0 fA cm^{-2} (n+/p junction) are reached. Efficient current extraction is presented with specific contact resistivities of 86 mΩ cm^2 on n-type wafer and 19 mΩ cm^2 on p-type wafers, respectively. High-resolution transmission electron microscopy reveals that the layer stack consists of intermixed SiO_x and Si phases with the Si phases being partly crystalline already in the as-deposited state. Thermal annealing at temperatures $\geq$ 850 °C further promotes crystallization of the Si-rich regions. The addition of the SiO_x phase enhances the thermal stability of the contact and should allow to tune the refractive index and improve transparency, while still providing efficient electrical transport through the crystalline Si phase, which extends throughout almost the entire contact.

1. Introduction

Crystalline silicon (c-Si) solar cells have a market share of > 90% [1] and represent the most mature and promising photovoltaic technology to replace fossil fuels and nuclear energy sources. In most c-Si solar cells the Si wafer is in direct contact with the metallization, forming a metallurgical c-Si/metal junction. The direct metal-silicon interface is affected by very high recombination rates, resulting in a decrease of the solar cell's photovoltage and therefore energy conversion efficiency [2]. This voltage loss can be overcome by inserting passivating buffer layers between the silicon wafer and the metal contact. First approaches, based on thin silicon oxide buffer layers capped with doped poly-silicon or semi-insulating poly-silicon (SIPOS) were pioneered already in the 1980s [3–5]. Recently, impressive solar cell results were demonstrated using a similar approach as rear contact [6–9], with associated recombination current at the rear side of only 7 fA cm^{-2} [10]. This contact structure is based on a very thin SiO_2 buffer layer coated by a highly doped silicon layer. During a thermal annealing step at typically 800–900 °C, dopants diffuse from the deposited silicon layer into the wafer forming a highly doped region. Afterwards, a hydrogenation step [11]

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http://dx.doi.org/10.1016/j.solmat.2016.06.040
0927-0248/

is applied to chemically passivate electronic defects at the wafer-SiO_2 interface to "switch on" the passivation [6].

With the excellent quality of poly-Si junctions employed as rear contact, the front side contacting scheme becomes the efficiency limiting element [10]. Consequently, in order to further increase the solar cell efficiency, passivating contacts are also needed at the front side. While requirements for a full-area passivating front contact are similar to these for the rear contact in terms of passivation behavior and electrical transport, the front contact layer stack also has to be optically highly transparent to avoid parasitic absorption losses. This can be achieved with thin and highly crystalline silicon layers since the absorption coefficient of crystalline silicon in the visible and infrared is much lower than that of amorphous silicon. Full crystallization of thin Si layers can be reached by prolonged thermal annealing [12]. This might, however, lead to deteriorated surface passivation due to rupture of the SiO_x buffer layer [6,13–15]. Alternatively, thicker SiO_2 buffer layers can be used [5,7], but this approach requires a "SiO_2 break up" step at 1050 °C which might degrade surface passivation or alter the doping profile in an unwanted way. To overcome these limitations, we propose to choose deposition regimes that result in crystalline structures in the film already before thermal annealing, such that moderate temperatures (700–900 °C) are sufficient to achieve almost full crystallization.

To further decrease optical absorption we introduce a high band gap material, namely silicon oxide, as a matrix around the silicon crystallites. The added SiO_x phase gives the opportunity to tune the refractive index of the mixed-phase material [16]. The concept of Si phases embedded in a SiO_x matrix is related to the early work on SIPOS-based junctions [3,4,17,18]. SIPOS is a homogeneous material with Si inclusions surrounded by SiO_2 phases and features rather high specific resistances due to the transport barrier caused by the Si/SiO_2 band offsets.

In contrast to SIPOS like approach, we propose in this paper a layer structure in which the Si phases extend as pillars or filaments from one side to the other of the layer, thus enabling efficient current transport across the layer. We present an electron-selective passivating junction layer stack consisting of a phosphorus-doped nc-SiO_x/nc-Si double layer on top of a chemical oxide, prepared by plasma enhanced chemical vapor deposition (PECVD) and a thermal annealing step. The contact is investigated as n+/n and as n+/p junction using both n- and p-type wafers, respectively. We discuss the effect of annealing dwell temperature on passivation properties and nanostructural transformations.

2. Experimental

The investigation of the passivating electron contact was done using symmetrical structures based on 280 μm thick double side polished 4-inch (100) 2.8 Ω cm silicon wafers doped with phosphorus or boron (Fig. 1). After cleaning using standard wet chemistry, a 1.2 nm thin SiO_x layer was formed by wet chemical oxidation [19,20], also referred to as "chemical SiO_x". Subsequently, a phosphorus-doped SiO_x/Si bilayer structure was deposited by PECVD on both sides. The individual layers are also referred to as "deposited SiO_x" and "deposited Si" in order to distinguish from the chemical SiO_x. The samples were then annealed for 15 min in nitrogen (N_2) atmosphere at temperatures from 750 °C to 950 °C. This was followed by a 30 min forming gas (4% H_2 in N_2) anneal at 500 °C to passivate electronic defects at the wafer-SiO_x interface. The effective minority carrier lifetime was measured by photoconductance decay and the method of Kane and Swanson [21] was applied to extract the emitter saturation current density at an excess carrier density of $1 \cdot 10^{16}$ cm^{-3}. The spatial homogeneity of the passivation was analyzed using photoluminescence imaging (PLI). The doping profile was analyzed by secondary ion mass spectroscopy (SIMS) with a Cameca ims 4f-E6. For electrical characterization, coplanar aluminium (Al) contacts were thermally evaporated, and the specific contact resistivity was measured using the transfer length method (TLM). Crystallization of the Si phases and stress in the layer was characterized by Raman spectroscopy. Care was taken to suppress the signal of the silicon wafer in order to get a clear signal only from the deposited layers. This was done using a 442 nm laser, which has a Raman collection depth of only around 150 nm in c-Si [22], and additionally by polarizing the laser in such a way that the signal from the underlying wafer was minimized [23].

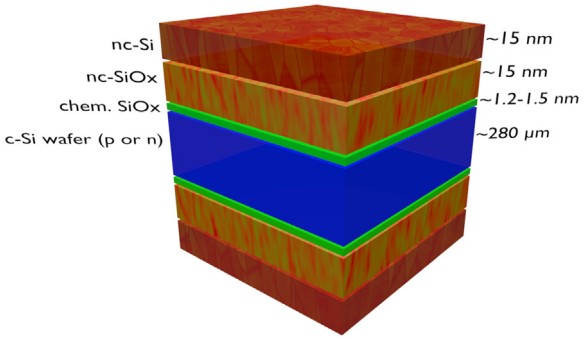

Fig. 1. Schematic of the symmetrical samples with the nc-SiO_x/nc-Si carrier-selective junction stack. The mixed-phase layer is indicated by silicon phases (red) embedded in an oxide matrix (green). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

The structural changes were further characterized by transmission electron microscopy (TEM) in an FEI Titan Themis. The microscope was operated at 300 kV for experiments involving high-resolution (HR) TEM and scanning TEM (STEM) high-angle annular dark field (HAADF) imaging combined with energy-dispersive X-ray spectroscopy (EDX) and at 200 kV for STEM electron energy-loss spectroscopy (EELS) measurements, which were performed with a convergence of 28 mrad and a similar collection angle using a Gatan GIF Quantum ERS high energy resolution EELS spectrometer and energy filter (dispersion of 0.1 eV per channel). To this purpose, TEM lamellae were prepared from samples that were either as-deposited or annealed at 850 °C or 900 °C using the conventional focused ion beam (FIB) lift-out technique in a Zeiss Nvision 40.

3. Results and discussion

3.1. Surface passivation

We investigated the effect of the additional silicon oxide phase in our deposited passivating layer stack by varying the deposition time of the nc-SiO_x layer while keeping the total deposition time of the nc-SiO_x/nc-Si stack constant. The implied open-circuit voltage iV_{OC} and the emitter saturation current J_0 after annealing at 900 °C are plotted in Fig. 2a for n-type wafers. The surface passivation is clearly enhanced with increasing nc-SiO_x thickness.

Additionally, we tested the tolerance of our contact structure to variations of dwell temperature for the case of a stack with 36% nc-SiO_x relative deposition time. The dependence of iV_{OC} and J_0 on annealing dwell temperature is shown in Fig. 2 for n+/p junctions (b) and n+/n junctions (c). Excellent surface passivation is achieved for temperatures above 850 °C up to 950 °C for both n- and p-type wafers. In other studies, where the doped Si layer was deposited directly on the chemical SiO_x buffer layer, a degraded surface passivation was reported for annealing temperatures