CdS and $Zn_{1-x}Sn_xO_y$ buffer layers for CIGS solar cells

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ABSTRACT

Thin film solar cells based on Cu(In,Ga)Se₂ (CIGS), where just the buffer layer is changed, were fabricated and studied. The effects of two different buffer layers, CdS and $Zn_xSn_{1-x}O_y$ (ZnSnO), are compared using several characterization techniques. We compared both devices and observe that the ZnSnO-based solar cells have similar values of power conversion efficiency as compared to the cells with CdS buffer layers. The ZnSnO-based devices have higher values in the short-circuit current (J_{sc}) that compensate for lower values in fill factor (FF) and open circuit voltage (V_{oc}) than CdS based devices. Kelvin probe force microscopy (KPFM) results indicate that CdS provides junctions with slightly higher surface photovoltage (SPV) than ZnSnO, thus explaining the lower V_{oc} potential for the ZnSnO sample. The TEM analysis shows a poly-crystalline ZnSnO layer and we have not detected any strong evidence of diffusion of Zn or Sn into the CIGS. From the photoluminescence measurements, we concluded that both samples are being affected by fluctuating potentials, although this effect is higher for the CdS sample.

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1. Introduction

Thin film solar cells based on Cu(In,Ga)Se₂ (CIGS) have recently achieved a certified power conversion efficiency of 22.8% [1], which is a significant increase from the 2013 value of 20.4% [2]. This recent improvement was achieved by the development of a new process on the CIGS surface consisting of evaporating KF after the growth of the CIGS layer and prior to the deposition of the buffer layer. Its full effects are still being studied but it has been shown that this process creates a CIGS/buffer junction with better properties by increasing the solar cell open circuit voltage, V_{oc}, and fill factor, FF [3]. The highest performance CIGS solar cells were achieved with a buffer layer consisting of CdS deposited by chemical bath deposition (CBD). However, CdS as a buffer layer exhibits some intrinsic problems: i) low bandgap energy, ~2.4 eV, that prevents high energy photons from arriving to the CIGS; (ii) it contains the toxic element Cd; and (iii) it is deposited with a non-vacuum method which is not favourable since the processes that are made before and after the buffer layer deposition are vacuum-based [4]. The ideal buffer layer should have: (i) electrical properties as good as the ones of CdS, if not better; (ii) a higher bandgap energy than the one of CdS; (iii) contain only non-toxic

elements; and (iv) allow deposition by a vacuum compatible technique. Many Cd-free materials have been proposed and studied [4]. However, the resulting solar cells usually lag behind CdS solar cells in terms of V_{oc} and FF; for example, the previous world record solar cells achieved a value of 21.7% with CdS but only 21% with Zn(S,O) [5]. Solar cells with Cd-free buffer layers usually achieve higher values of short circuit current, J_{sc}, due to their higher band gap energy compared with CdS. In this paper we focus on the alternative buffer material $Zn_{1-x}Sn_xO_y$ (ZnSnO). Solar cell devices with a ZnSnO buffer layer have achieved values of power conversion efficiency above 18% and performing on the same efficiency level as CdS [6–8]. These results are quite promising, nevertheless further studies are needed for a better understanding of this material and to identify if it imposes the same benefits to the CIGS as CdS buffer layers.

In view of the recently shown importance of the front interface and the general search for Cd-free buffer layers, in this work, we performed a comparison between CIGS devices prepared with CdS and with ZnSnO buffer layers. Several techniques were used to assess the differences between the electrical behaviour of devices with CdS or with ZnSnO buffer layers. We would like to emphasize that in this study we used CIGS grown using an in-line and semi-industrial pilot tool evaporator. These processes are very similar to industrial ones: (a) the substrates are glasses without diffusion barriers [9]; (b) the Mo layer is thin to cut costs and deposited in a batch reactor with no control over its oxidation [10]; (c) the CIGS

was grown in a batch reactor on large substrates (12.5 × 12.5 cm) [8]; (d) the TCO layers are thick; and (e) no anti-reflective (AR) coatings are used.

2. Experimental

2.1. Materials preparation

Solar cells with the structure soda-lime glass(SLG)/Mo/CIGS/ buffer/i-ZnO/ZnO:Al/Ni-Al-Ni-grid without AR coating were prepared at Uppsala University using the Ångström solar cell baseline [8]. CIGS was prepared in an in-line evaporator using a one stage co-evaporation process [8]. The positioning of the sources resulted in a linearly decreasing [Ga]/([Ga]+[In]) ratio from the back contact to the front of the film [11] and a detailed characterization of this type of profile can be found elsewhere [11]. The tool co-evaporates CIGS on 12.5 × 12.5 cm^2 substrates. The composition of the CIGS used in this study was [Ga]/([In]+[Ga])=0.42 ± 0.03 and [Cu]/([In]+[Ga])=0.86 ± 0.03. The thickness was measured to be 1.85 ± 0.25 μm, using a PANalytical Epsilon 5 X-ray fluorescence (XRF) system with a CIGS calibration sample. In addition, elemental depth profiles of the CIGS layer were recorded with glow discharge optical emission spectroscopy (GDOES) in a Spectruma GDA750 (Spectruma Analytik GmbH, Germany) [12]. The composition and thickness values of the GDOES measurements were integrated/corrected using the XRF values. A single substrate was split so that part was covered with CdS, whereas another part was covered with ZnSnO, thus our devices are based on the same CIGS. Additionally, this step ensures that both the handling of the glass substrate prior to deposition and the Mo layer are the same for the compared devices. After the buffer deposition the same solar cell processing was done on both samples consisting of sputtering of i-ZnO and ZnO:Al, e-beam evaporation of Ni/Al/Ni grids, and scribing. In that way 12 solar cells were fabricated for each buffer layer. For the characterizations that needed non-finished solar cells, i.e. SLG/Mo/CIGS/buffer, additional pieces of the sample were used where the processing finished right after the deposition, as shown in Fig. 1. To prevent any possible degradation of the materials, storage, transport, and shipping of all samples, were made either in low-vacuum, or in a dry N$_2$ environment.

CdS was deposited by conventional CBD with a solution of 1.1 M ammonia, 0.100 M thiourea, and 0.003 M cadmium acetate. The solution is mixed in a beaker at room temperature, and the samples are immersed into the beaker, which is subsequently heated to 60 °C in a water bath. During the growth process, the solution is stirred for 10 s each minute. The baseline process time is 8 min and 15 s, and the samples are then directly removed from the CBD beaker and immersed in clean deionized water to stop the growth process. This process typically produces films with a thickness of 50–70 nm. For the photoluminescence measurements, CdS was etched using a 5% HCl solution during 30 s. The estimated

time interval between the etching and the mounting of the sample in the cryostat, in helium atmosphere, was minimized, circa 5 min, in order to avoid the degradation of the CIGS layer [13,14].

The ZnSnO buffer layer was grown by using a Microchemistry F-120 ALD reactor kept at a deposition temperature of 120 °C according to a previously developed process [6]. As precursors, diethyl zinc (DEZn or Zn(C$_2$H$_5$)$_2$), tetrakis (dimethylamino) tin (TDMASn or Sn(N(CH$_3$)$_2$)$_4$), and deionized water (H$_2$O) were used together with nitrogen gas (N$_2$) as carrier and purge gas. A total of 625 ALD cycles were deposited, where the pulse lengths were 400/400:800:400:800 ms long for the Sn/Zn precursor:N$_2$:H$_2$O:N$_2$ pulses, respectively. The [Sn]/([Sn]+[Zn]) pulse ratio was set to 0.4 in order to produce a buffer layer with an x-value of around 0.2.

2.2. Characterization techniques

Completed solar cell devices were characterized by current density-voltage (J-V) measurements with illumination from an ELH lamp. Values of FF, J$_{sc}$, V$_{OC}$, and power conversion efficiency were extracted from the J-V curves as well as other parameters as explained elsewhere [15]. The shown values are averages of 12 cells together with its standard deviation. External quantum efficiency (EQE) was determined under ambient light, using chopped monochromatic light that was scanned through the wavelength interval of 360–1200 nm in 2-nm steps. To obtain the capacitance-voltage, C-V, characteristics, an Agilent 4294A impedance analyser with a DC voltage sweep range between − 1.0 V and + 0.6 V using 0.1 V steps and a frequency of 10 kHz with an AC modulation voltage of 50 mV rms was used. These measurements were performed at room temperature and in dark conditions. After the sample preparation and electrical characterization the samples were transferred to INL for further investigations.

Scanning transmission electron microscopy (STEM) images were taken with a FEI Titan Themis 80–300 kV Cs-probe corrected transmission electron microscope, operating at 300 kV accelerating potential and equipped with an EDS-Bruker silicon drift detector. In this method a coherent focused probe scans across the specimen and the X-ray emission spectrum is recorded in each probe position. Conventional high resolution transmission electron microscope (HRTEM) images were taken with a Jeol JEM 2100 80–200 kV operating at 200 kV. The lamellas were prepared in a focused ion beam (FIB) FEI Dual-Beam Helios 450S with FIB Cu-grids using a technique known as "lift-out" [16]. On top of the buffer layer we deposited a protective Pt bi-layer using the electron beam and the Ga beam. The ZnSnO lamella was ion milled to a high extent and thus the second Pt layer is not seen, such detail does not cause differences in the interpretation of the results shown here. Despite using the Ga ion beam with low energy (2 keV) in the final polishing to remove amorphous Ga, this layer is significantly reduced. However we cannot say that this layer is completely removed on the samples and therefore the Ga counts
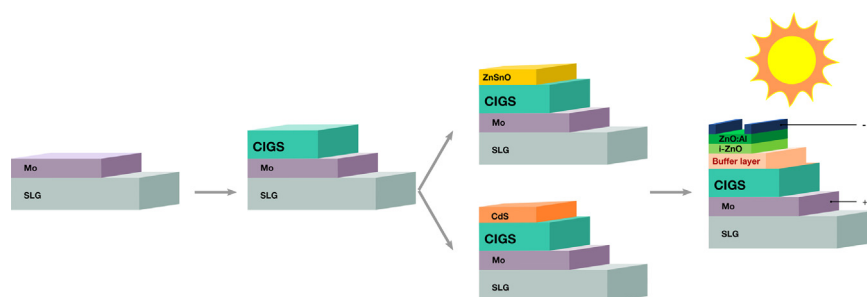

Fig. 1. Representation of the fabrication and design of experiment. In the process of fabricating of the solar cell, the only step where the devices were not processed at the same time was the buffer layer deposition.