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Printed interconnects for photovoltaic modules

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ABSTRACT

Film-based photovoltaic modules employ monolithic interconnects to minimize resistance loss and enhance module voltage via series connection. Conventional interconnect construction occurs sequentially, with a scribing step following deposition of the bottom electrode, a second scribe after deposition of absorber and intermediate layers, and a third following deposition of the top electrode. This method produces interconnect widths of about 300 µm, and the area comprised by interconnects within a module (generally about 3%) does not contribute to power generation. The present work reports on an increasingly popular strategy capable of reducing the interconnect width to less than 100 µm: printing interconnects. Cost modeling projects a savings of about $0.02/watt for CdTe module production through the use of printed interconnects, with savings coming from both reduced capital expense and increased module power output. Printed interconnect demonstrations with copper-indium-gallium-diselenide and cadmium-telluride solar cells show successful voltage addition and miniaturization down to 250 µm. Material selection guidelines and considerations for commercialization are discussed.

1. Introduction

Film-based photovoltaic (PV) technologies, such as cadmium telluride (CdTe), copper-indium-and copper-indium-gallium-diselenide (CIS and CIGS), amorphous silicon, and the various types of organic polymer: fullerene systems (e.g. P3HT: PCBM), employ monolithic interconnects (ICs) to add the voltage between cells in modules. Conventional IC construction occurs sequentially, with a scribing step following deposition of the bottom electrode, a second scribe after deposition of absorber and intermediate layers, and a third following deposition of the top electrode – the so-called P1, P2, and P3 scribes, respectively (Fig. 1). The area comprised by ICs does not contribute to power generation, and therefore, a trade-off applies between the module geometric fill-factor and the IC width. A module with narrower ICs contains more active area, and therefore generates more power. The present work reports on an increasingly popular strategy to reduce the IC width and at the same time streamline module assembly: printing ICs. Consider the cumulative impact of 300 µm wide ICs on a module with cell width of 1 cm (characteristic for CIGS and CdTe PV): this amounts to 3% dead area; for a 200 W module more than 5 W of possible energy generation is forgone.

Previously, IC width reduction has been achieved by reducing the width of individual scribe lines. Here, transitioning from ns-pulsed lasers to ps-pulsed lasers for ablation provides advantages, enabling both narrower and more uniform scribing due to reduced thermal effects [1–5]. This also reduces unintended deposition of ablated materials on scribe sidewalls, which unmitigated create shunting pathways [4,5]. Other authors report IC width down to 250 µm using a combination of pulsed-laser and optimized mechanical scribing [6]. Additional IC width reduction was achieved by replacing P2 and P3 mechanical scribing with ps-laser scribing. In this way other researchers achieve IC widths down to 200 µm [3,7]. These approaches will provide short-term improvements for thin-film PV manufacturers (current IC width ~ 300 µm). However, to go below 200 µm will likely require alternative IC architectures, and the printed IC approach provides the means.

Although Thalheimer patented the original printed IC process almost 30 years ago, the method only recently finds traction in mainstream PV manufacturing [8]. Renewed interest in printing the ICs is evidenced by numerous patents filed in the last several years in this area [9–12] and multiple developmental efforts launched by collaborative technology consortiums [13,14]. The increased attention follows key advances in direct-write, printed-electronics technologies in the last several decades. Commercially available low-temperature
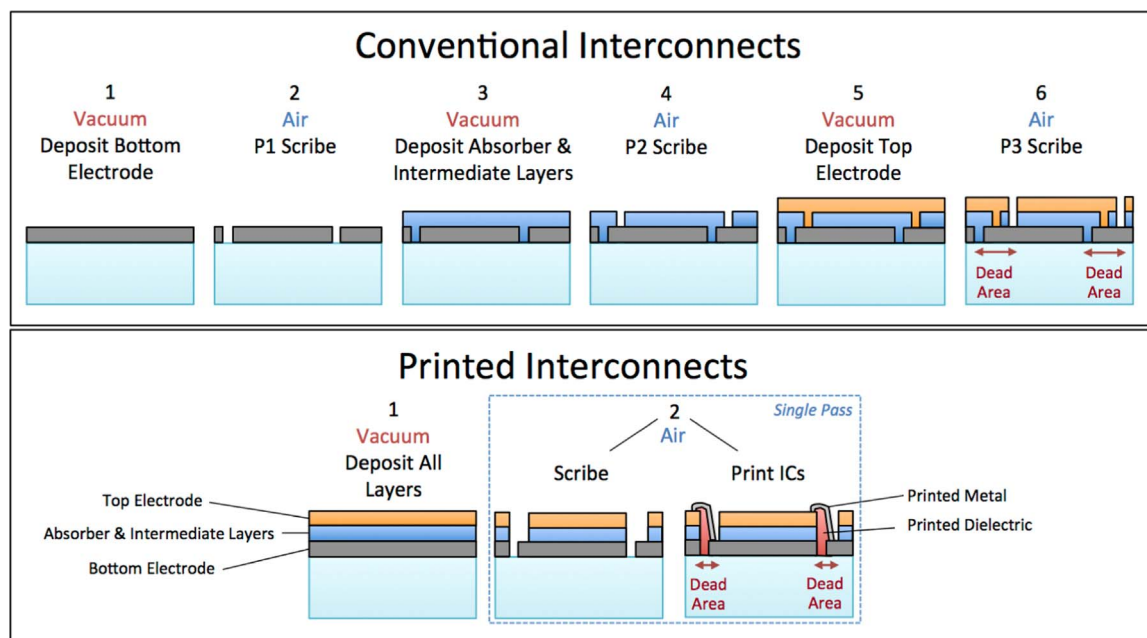

Fig. 1. Process sequence for monolithic cell integration using (top) conventional vs. (bottom) printed interconnects (2-scribe geometry depicted).

(less than 200 °C) and UV-curable inks enable deposition of conductive and dielectric IC features with minimal thermal-induced degradation of solar cell materials, improved printing resolution (feature size down to 20 µm) allows IC patterning with minimal shading, and industry relevant deposition rates now provide the means for implementation of direct-write processes in high-volume manufacturing [15,16]. Couple these improvements with a modern laser-scribing practice, and printing ICs with non-traditional architectures becomes a viable option.

In addition to providing higher geometric fill-factor, printing ICs after deposition of all solar cell layers provides many other advantages. For one, performing one scribing/interconnection step, as opposed to performing three separate P1-, P2-, P3-scribing steps at different stages of the solar module production sequence, eliminates 2 process steps and streamlines production. Integrated scriber/printer instruments, such as those reported in Refs. [10,14] can accomplish this. The method also eliminates venting and pumping time delays between vacuum-/atmospheric-pressure-based process steps associated with ex-situ transfers in the conventional process (see Fig. 1), wherein exposure to air between deposition steps can degrade cell performance, such as by oxidation for example. Thus, enabling complete cell deposition under vacuum before transferring to atmosphere for scribing may also enable additional power gains. Lastly, in the case of CIGS, since the Mo is freshly exposed for interconnection in a printed IC process, parasitic contact resistance between the TCO and molybdenum (Mo) bottom electrode associated with a deleterious molybdenum-diselenide intermediate layer is avoided [17]. Hence, printing the ICs provides numerous paths to power gains.

This work focuses on material selection considerations for printing ICs, and the expected impact of implementing a printed IC process on CdTe PV module manufacturing costs. Printed IC demonstrations with both CIGS and CdTe modules show that this strategy can be applied to both substrate and superstrate configuration solar cells, analogously. Cost modeling weighs expected benefits of printed ICs against estimated capital investment required to implement a printed IC process in CdTe PV manufacturing. Calculations project a savings of about $0.02/watt. Key in favorable manufacturing economy is higher module power with comparable capital expense since the additional cost of printing equipment is offset by savings achieved by reducing the number of steps and eliminating ex-situ transfers.

2. Printed interconnect architectures

Numerous IC architectures, including the conventional 3-scribe form, are possible through the use of a printed dielectric and printed metal to make series connections between cells. A printed 3-scribe IC (Fig. 2(top)) is made by performing a P1-scribe through the full stack, P2- and P3-scribes down to the bottom electrode, and then depositing dielectric and metal into the scribes. Here, the dielectric printed into the P1 scribe isolates the bottom electrode upon subsequent metallization to make the series connection between two cells. However, examining the printed 3-scribe IC form, with printed dielectric and metal features separated by absorber/TCO stack margins, one recognizes the P1/2 and P2/3 margins need not be maintained to make the electrical series connection and also maintain electrical isolation of top and bottom electrodes. Fig. 2(middle) shows a 2-scribe IC architecture (demonstrated in Section 4), made by performing a P1-scribe through the full stack, a P2-scribe to expose the bottom electrode, and then printing carefully so as to maintain the margin between the printed metal and the P2-scribe side-wall. Ultimately, with sufficient control over the dielectric and metal printing resolution, and with optimal alignment of the deposition to the P1-scribe, a single-scribe IC should be possible. This concept is shown in Fig. 2(bottom). While the single-scribe IC remains an elusive goal experimentally, it should be possible in principal.

With increasingly narrow scribe-widths possible using new ultrafast lasers (scribe widths approaching 10 µm [3]), and improved industrial printing capabilities, the opportunity to integrate scribing and printing tools to reduce the 3-scribe IC structure width to 250 µm becomes attainable. In the case shown in Fig. 2(top) the IC-width is limited by scribe widths of ~ 50 µm, P1/2 and P2/3 margin widths of 40 µm, and printed feature width down to 70 µm. Here, 40 µm wide margins suffice, as opposed to wider margins on the order of 100 µm wide in conventional IC's, since the scriber and printer are integrated in a printed-IC process, which reduces the risk of shunting. IC width approaching 100 µm should be attainable by printing ICs with simplified architectures. Fig. 2(middle) shows the feature sizes needed to construct a 2-scribe IC with total width of just 120 µm, adding more than 100 µm of active cell width. Despite limitations on the ablation process quality in the present work, discussed in Section 4, IC-widths down to 250 µm could still be obtained using a variation on the 2-