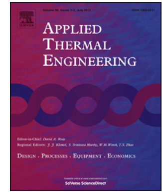
Applied Thermal Engineering 56 (2013) 176–184

Contents lists available at SciVerse ScienceDirect

Applied Thermal Engineering

journal homepage: www.elsevier.com/locate/apthermeng



Determination of temperature distribution in three-dimensional integrated circuits (3D ICs) with unequally-sized die

Leila Choobineh, Ankur Jain*

Mechanical and Aerospace Engineering Department, University of Texas, Arlington, 500 W First St, Rm 211, Arlington, TX 76019, USA

HIGHLIGHTS

- A model is developed for the three-dimensional temperature field in unequally-sized 3D integrated circuits.
- Model results are in excellent agreement with finite-element simulation models.
- Model enables a fundamental understanding of thermal management challenges in 3D ICs.
- An unequally-sized 3D IC has higher temperature rise than equivalent uniform 3D IC due to thermal constriction/spreading.

ARTICLE INFO

Article history:
Received 23 October 2012
Accepted 6 March 2013
Available online 18 March 2013

Keywords:
Three-dimensional integrated circuits (3D ICs)
Unequally sized die
Fourier series expansion
Floorplanning
Semiconductor devices

ABSTRACT

There is much interest in 3D integrated circuits (3D IC) technology for vertical integration of multiple device planes in semiconductor devices. Stacking several device planes vertically offers significant electrical performance improvements. This can also lead to reduced design and manufacturing costs. Several 3D IC manufacturing and packaging approaches require adjacent die sizes to be different from one another since this facilitates differentiated manufacturing and design. However, it is expected that unequally-sized die may cause deteriorated thermal performance due to heat spreading and constriction. This manuscript presents a heat transfer model for predicting the three-dimensional temperature field in a multi-die 3D IC with unequally-sized die. This problem is solved iteratively using solutions of three simpler heat transfer problems outlined in the manuscript. Temperature fields predicted by the model are in close agreement with finite-element simulation results. The model is used to compare the thermal performance of unequally-sized die stacks with a uniformly-sized die stack. Results indicate that the greater the degree of non-uniformity in the die stack, the greater is the peak temperature rise. The model and results presented in this manuscript are expected to aid in the development of effective thermal design tools for 3D ICs.

© 2013 Elsevier Ltd. All rights reserved.

1. Introduction

Three-dimensional integrated circuits (3D IC) technology refers to the vertical integration of circuits on multiple semiconductor substrates [1,2]. 3D ICs offer several advantages over traditional microelectronic designs, including heterogenous design integration, reduced interconnect delay, etc. [3,4]. It has been estimated that 3D integration provides roughly the same performance benefits as dimensional scaling by one technology node without the prohibitive associated costs [5–7]. Vertical integration is usually implemented by bonding of metal pads on frontside or backside of adjacent die, which in addition to mechanical adhesion also provide a pathway for electrical communication between the die [3]. 3D IC technology also often necessitates signal transmission from one face of a die to the other. This is usually implemented using through-silicon vias (TSVs), which are metal-filled vias etched all the way through the substrate [7].

Thermal management of 3D ICs has been widely recognized as a significant technology challenge for widespread implementation of this technology [6,8–10]. Like traditional microelectronic chips, temperature rise and temperature uniformity is a concern in 3D ICs, since temperature and thermomechanical stresses generated due to temperature differential both adversely affect transistor performance. Thermomechanical stresses also adversely affect chip–package interactions and reliability. While the back face of the die was traditionally available for heat removal, for example by attachment to a heat sink using a thermal interface material, both faces of the die on a 3D IC are utilized for electrical interconnection

* Corresponding author. Tel.: +1 817 272 9338; fax: +1 817 272 2952.
E-mail addresses: jaina@uta.edu, ankurjain@stanfordalumni.org (A. Jain).

1359-4311/$ – see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.applthermaleng.2013.03.006

Nomenclature

Symbols

a,b,c	die dimensions
d	coefficient
h	Heat transfer coefficient ($Wm^{-2}K^{-1}$)
k	thermal conductivity ($Wm^{-1}K^{-1}$)
n,m	indices for infinite series solutions for temperature rise
p	coefficient
Q	heat flux (Wm^{-2})
T	temperature rise (K)
x,y,z	spatial coordinates (m)

Subscript

g	guessed temperature field
i	Die number

with adjacent die. The heat removal challenge is particularly exacerbated for die in the middle of the vertical stack. Early work in this field focused on investigation of thermal management challenges in 3D ICs [11,12] and the thermal implications of various electrical design models being considered for 3D IC technology [13,14].

Thermal envelope available for 3D IC design has been estimated by modeling changes in block-level power consumption due to three-dimensional design and its impact on thermal management [15]. A number of thermal management approaches have been investigated for meeting the heat dissipation challenge in 3D ICs [16–20]. These approaches include liquid cooling [16–19], thermoelectrics-based cooling [20], etc. A limited amount of experimental work on measurement of thermal characteristics of 3D ICs has also been reported in the past few years [21–24]. Recent work has reported the use of a novel thermal lid for thermal management of unequally sized die stack [36].

While most of the thermal modeling work for 3D ICs has assumed identically sized die [9,25–28], manufacturing and packaging considerations often require that the die size not be the same [6]. For example, making the bottom die larger than the top die allows wire bond connections to be made to the exposed area of the bottom die. Further, by employing die-on-wafer bonding, significant yield improvement can be obtained without requiring the die to be the same size [6]. Finally, having unequally sized die is also necessitated by implementation of heterogenous design. For example, the same memory die designed using a pre-specified bond pad layout could be implemented on multiple logic die designs for different applications, none of which need to necessarily be the same size [4]. The memory die does not need to be designed for each application separately, resulting in significant reduction in cost and design time.

The nature of heat transfer in unequally-sized die is inherently different from a stack of identical die due to heat spreading and constriction. A variety of thermal simulation approaches including finite-difference and finite-element modeling have been employed for determining the temperature field in a 3D IC [26,27,29,30]. Analytical heat transfer models developed for uniformly-sized die [31–33] are not applicable if the die sizes are not uniform. Edge effects, which are usually neglected in the analysis of identical die may be important for unequally-sized die. Past work on heat spreading and constriction in electronic packages has only considered two layers of unequally-sized substrates [34]. Another paper reported finite-difference modeling of heat conduction in unequally-sized 3D IC stacks [35]. While such approaches help determine the temperature profile in a 3D IC, a more fundamental approach involving analytical solutions of the governing energy equations would help develop a basic understanding of thermal management of unequally-sized 3D IC stacks, and how such stacks differ from uniformly-sized stacks. Given the growing interest in thermal management of 3D ICs in general, and unequally-sized die stacks in particular, it is essential to develop a fundamental understanding of this problem and derive analytical expressions for the temperature field based on solutions of the governing energy equations. Such approach is likely to help improve thermal design of 3D ICs.

This paper presents an analytical model for understanding heat transfer characteristics of a stack of unequally sized die with non-uniform heating on each die. Governing energy conservation equations with appropriate boundary conditions are solved, resulting in three-dimensional temperature fields for each die. The non-uniform die size presents interesting modeling challenges, necessitating an iterative approach for determining the temperature field. Results are in close agreement with finite-element simulations. The model is used for comparing the thermal performance of non-uniform 3D ICs with a uniformly-sized 3D IC. It is found that the larger the degree of non-uniformity in die size, the higher is the temperature, due to additional thermal spreading/constriction resistance. This work provides a useful tool for understanding the fundamentals of heat transfer in 3D ICs and evaluating the realistic thermal impact of 3D integration.

2. Steady-state heat conduction model for non-uniformly sized 3D IC

The die stack consists of N dies, each of which is a cuboid of size a_i by b_i by c_i. Fig. 1 shows the x-z cross-section of the geometry under consideration. All dies in the stack are assumed to be centered around a common axis. The model presented in this manuscript can also be used for non-concentric die stacks with appropriate transformations in the x and y axes. A heat sink is attached to the bottom-most die, which is modeled using a convective boundary condition. It is assumed that the top-most die is connected to the electrical package, heat loss through which is neglected. This is a reasonable assumption because of the presence of the mother board and other electrical units on the package end

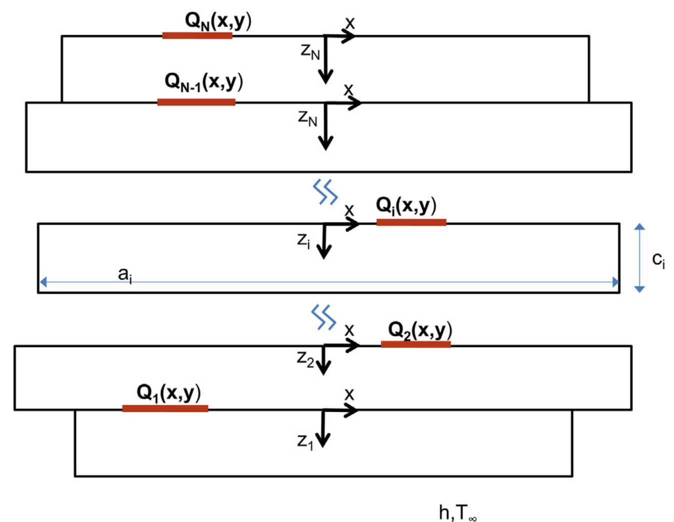


Fig. 1. Schematic of the cross-section view of the N-die stack comprising unequally sized die. The size of the ith die in the direction perpendicular to the paper is b_i. All die are assumed to be concentric, and the origin of coordinates for each die is assumed to be located at the center of the top x–y plane of the die.

Download English Version:

https://daneshyari.com/en/article/646972

Download Persian Version:

https://daneshyari.com/article/646972

Daneshyari.com