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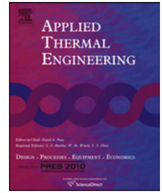

Thermal conduction analysis and characterization of solder bumps in flip chip package

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ABSTRACT

Flip chip has been widely used in microelectronic packaging to meet the requirements of high density and optimal performance. With the shrinking of the package size, the heat dissipation problem is getting more serious, and the thermal modeling and measurement of flip chip have become hot topics. This paper investigated the thermal performance of the solder bumps using analytical and numerical methods. A lumped thermal resistance network was derived from the mathematical model of heat transfer in the flip chip structure. Common defects were introduced in the 3D finite element model. The impact of the defects on the heat conduction was investigated by the temperature distribution. The thermal performance of the solder bumps was characterized by using the thermal resistances. The relationship between the thermal resistance and the defects size was also studied, and the finite element model describes well the experimental data available from the literature. The results demonstrate that this model is effective for the thermal characterization of solder bumps, and can provide guidelines for failure detection in flip chip package.

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1. Introduction

Surface mounting technology plays an increasingly important role in microelectronic packaging. Flip chips (FC), ball grid array (BGA) and chip scale packages (CSPs) have been extensively used, in which solder bumps or solder balls are employed to interconnect the chip/package and the substrate. The solder bump technology provides decreased package size, greater I/O density and larger speed of signal propagation [1,2]. As the package scale continues to shrink, the chip power density increases dramatically, and the heat dissipation becomes a significant problem [3]. The inclusion of low-k materials also makes the situation deteriorate further. Excessive heat and large temperature gradients may introduce failures in the components [4]. Therefore, thermal modeling and measurement of flip chip packages have become hot topics recently in structure design and package reliability evaluation.

Thermal resistance is a principal index that indicates the thermal dissipation capability and is usually determined experimentally using an infrared (IR) technique, although the JEDEC electrical test method based on the JESD51-1 specification may also be used [5,6]. Due to the complexity of experiments for measuring thermal resistances, the finite element method (FEM) and finite volume method (FVM) are widely used in numerical analysis to perform thermal evaluation of the flip chip package. Chen et al. [7] proposed a finite element numerical methodology to predict the thermal resistance of FC-PBGA package, in which the empirically determined coefficients for convective heat transfer were applied on different exposed surfaces. Kandasamy et al. [8] constructed a CFD-based thermal model to investigate the thermal performance of the FC-CBGA package with and without a lid both in natural and forced convection environments. Joiner et al. [9] compared the thermal performances of flip chip packages between the plastic laminate substrate and ceramic substrate using finite element analysis. However, in these research the chip is regarded as a node, and the thermal resistances of junction-to-case, junction-to-board and junction-to-ambient are used to characterize the thermal performance of a given device package, as depicted in Fig. 1, while the internal structure of the package is neglected and the heat conduction via solder bumps or solder balls are not taken into consideration.

This study focused on the heat transfer analysis and thermal characterization of the solder bumps in flip chip package. The mathematical model of heat transfer in the flip chip structure is devised. A lumped thermal resistance network is derived from the simplified analytical model and the finite element method is used to evaluate the thermal performance of the solder bumps. The numerical code of COMSOL Multiphysics is adopted to perform the

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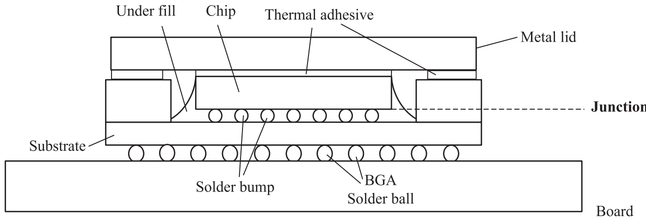

Fig. 1. Cross section of flip chip-BGA package.

thermal simulations. A three dimensional FEM model is initially constructed to predict the temperature distribution where defects of crack and void in solder bumps are also introduced. The heat dissipation capability of the solder bumps is assessed using the thermal resistance values, and the impact of defect size on the thermal resistance is also investigated using the FEM model.

2. Mathematical analysis of heat conduction in flip chip structure

Fig. 2 shows the schematic of the flip chip structure. The silicon die is attached to the substrate by a solder bumps array. The dimensions of the chip and substrate are $D1 \times D2 \times$ h and $S1 \times S2 \times r$, respectively. As known, the heat transfer in the solid body is governed by the Fourier diffusion equation, which describes the distribution and variation of temperature in a given region and time, and can be expressed as,

$$\frac{\partial T}{\partial t} = \frac{k}{\rho c_p}\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + \frac{Q}{\rho c_p} \tag{1}$$

where $T = T(x, y, z, t)$ depicts the temperature at the point (x, y, z) and time t, k denotes the thermal conductivity, ρ is the density and c_p the specific heat capacity, and Q is defined as the internal heat generation per unit volume in unit of w/m^3.

For the silicon die, assumed that the ith solder bump is located at the area of S_i, and the heat removal power is P_i, the boundary condition on the top and bottom surfaces can be written respectively as

$$\frac{\partial T}{\partial z}_{|z=h} = \begin{cases} \dfrac{P_i(t)}{k_d S_i} & \text{if}(x,y)\in S_i \\ 0 & \text{else} \end{cases} \tag{2}$$

and

$$\frac{\partial T}{\partial z}_{|z=0} = -\frac{\alpha}{k_d}\left(T_{top} - T_{amb}\right) \tag{3}$$

where k_d is the thermal conductivity of the silicon die, α is the heat transfer coefficient to environment, T_{top} is the value of $T(x,y,z,t)$ function on the top border, and T_{amb} denotes the ambient temperature.

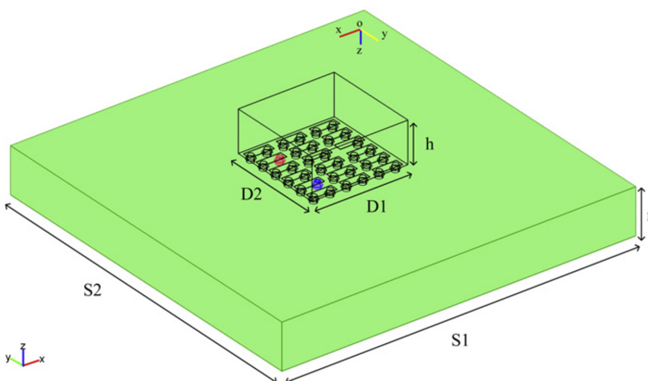

Fig. 2. Geometric model of the flip chip structure.

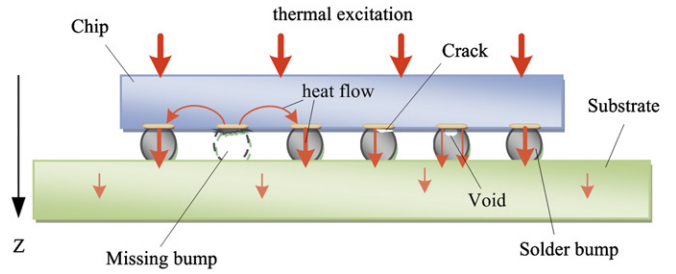

Fig. 3. One-dimensional heat transfer model.

The thermal removal from the side surface to ambient can be neglected due to the small dimension. The boundary condition for the side surface can be described as $\partial T/\partial x = 0, (x = 0, D1)$ and $\partial T/\partial y = 0, (y = 0, D2)$. We set the initial temperature as T_0, namely $T(x, y, z, 0) = T_0$.

For the substrate, we can express the boundary conditions and the initial temperature similarly. Therefore, the temperature at any point of the flip chip package can be described by the differential heat conduction equation (1). The heat exchange problem in the structure with single layered chip and substrate was solved analytically, and the temperature distribution was expressed in the linear expansion form along z coordinate [10]. Although it is proved to be valid, the solving process is rather complex.

In this paper, we put emphasis on the investigation of the heat conduction via solder bumps and the estimation of defects influence on the heat transfer in flip chip package. In the manufacturing environment there are no internal heat sources in the package since the chip is not in working condition. It is also assumed that all the materials are homogenous and an external thermal excitation is applied on the top surface of the chip, which ensures heating uniformity over all the solder bumps. To simplify the analytical process of heat exchange between the chip and the substrate, a one-dimensional heat transfer model is proposed as shown in Fig. 3. There are always some common defects in solder bumps [11], such as open, cracks, voids and missing solder bumps, some of

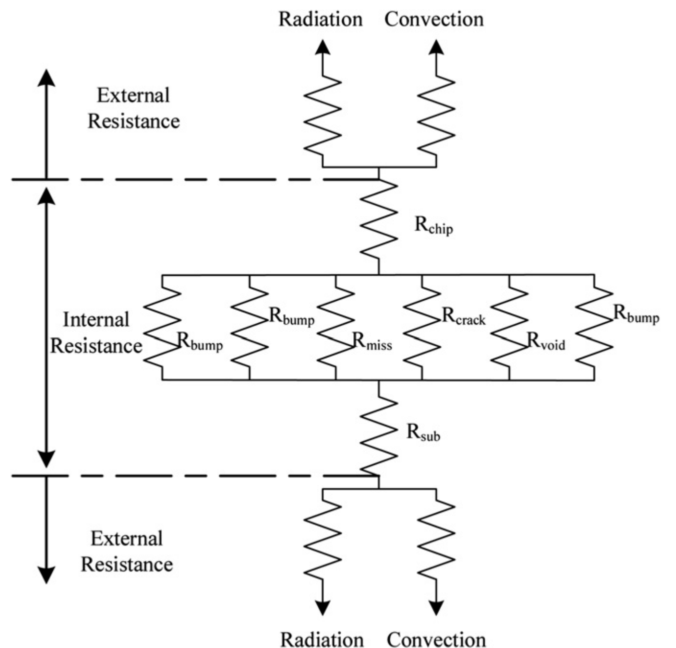

Fig. 4. Lumped thermal resistance network of the flip chip structure.

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